ADV7511

Low-Power HDMI 1.4 Compatible Transmitter with Audio Return Channel

PROGRAMMING GUIDE

- Revision G–

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Advantiv
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ANALOG DEVICES

REVISION HISTORY

Rev. 0:

Initial Release	

Rev A:

Section	Change Description
Section►4.3.2.1	Corrected register bit information for the "Input Style" bit
Sections►4.3.4, ►4.4.1.3, ►4.4.1.4, and►4.4.1.5	Clarified that automatic pixel repeat does not work with HBR, DSD, or DST audio inputs.

Rev B:

Section	Change Description
Section ►4.3.10	Added 3D section.
Section ►4.3.8	Updated CSC Tables.
Section►4.8	Updated reset information.
Section ►4.9	Updated CEC Timing Charts.

Rev C:

Section	Change Description
Section **5** -	Corrected recommended settings for fixed registers 0x98, 0x9C, 0x9D, 0xA2, and 0xA3.

Rev D:

Section	Change Description
Section ►4.3.8	Added additional CSC Tables
	Removed "confidential" statements

Rev E:

Section	Change Description
Section ►4.3.8	Added additional CSC Tables

Rev F:

Section	Change Description
Section ►4.7.1	Error controller register address corrected
Section ►Section 5 -	Changed chip revision to 12

Rev G:

Section	Change Description
Section ►4.3.8	Corrected CSC Tables 53 and 54

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SECTION 1 - INTRODUCTION

1.1 Scope and Organization

1.1.1 Organization

This document is intended to help a programmer understand the details of the operation of the ADV7511. It is divided into sections:

- **Section 2 -References**- is a list of other references, which will be helpful when designing with the HDMI Transmitter.
- **Section 3 -Quick Start Guide**- provides a reference to commonly used registers divided by function.
- **Section 4 -Programming Tasks**- is divided into common programming tasks. This section includes references to registers and detailed descriptions of the method to accomplish the task. For some tasks, the needed registers will be spread throughout the map, so this section helps the user locate the registers.
- **Section 5 -Register Maps**contains the complete register maps - The main register map contains cross-reference links to sections within the document that contain the relevant details on using each bit described.

1.1.2 Use of Register Bits

Different bits on a single byte may have various functions. ► Section 4 -Programming Tasks may refer to an isolated bit. Using a "read, modify, write" method when changing the value of these bits is recommended to guarantee that other bits in the register will not be affected. To find the functions of other bits in the byte, refer to ► Section 5 -Register Maps, where the Reference column points to the section with more detailed information about the register.

1.1.3 Register Types

Registers that do not have a defined functionality will be one of three types:

Fixed	Value may need to be set one time, but should never be changed.
Reserved	Register exists, but has no function.
Not Used	Register does not exist and will always be read back as 0. Any register not defined in the complete register map fits this description.

1.1.4 Format Standards

In this document, ADI has chosen to represent data in the following ways:

0xNN	Hexadecimal (base-16) numbers are represented using the "C" language notation, preceded by 0x.
0bNN	Binary (base-2) numbers are represented using "C" language notation, preceded by 0b.
NN	Decimal (base-10) numbers are represented using no additional prefixes or suffixes.
Bit	Bits are numbered in little-endian format; i.e., the least-significant bit of a byte or word is referred to as bit 0.

Bit descriptions in the register maps are assumed to be binary.

1.1.5 Links

There are many links in this document to help with navigation. Use a mouse click to follow a link, and use the Alt key + left arrow key to return.

1.1.6 Symbols

Symbols are used to indicate internal and external document references as follows:

- ► Indicates a reference to another section of this document.
- ▹ Indicates a reference to another document, either an ADI document or an external specification.

SECTION 2 - REFERENCES

2.1 ADI Documents

- ADV7511 Data Sheet
- ADV7511 Hardware User's Guide
- ADV7511 Software Driver User's Guide

2.2 Specifications

- EIA/CEA-861
- HDMI Specification 1.4
- HDCP 1.3
- IEC 60958
- IEC 61937
- The I 2C-Bus Specification

SECTION 3 - QUICK START GUIDE

The Quick Start guide brings attention to registers that need to be configured when initially bringing up the HDMI transmitter. For detailed information, refer to the section number link on the right side of the page. Complete registers and their descriptions are listed in ► Section 5 -Register Maps

Power-up the Tx (HPD must be high)	
0x41[6] = 0b0 for power-up – power-down	► 4.8
Fixed registers that must be set on power up	
0x98 = 0x03	► 4.2.9
0x9A[7:5] = 0b111	► 4.2.9
0x9C = 0x30	► 4.2.9
0x9D[1:0] = 0b01	► 4.2.9
0xA2 = 0xA4	► 4.2.9
0xA3 = 0xA4	►4.2.9
0xE0[7:0] = 0xD0	► 4.2.9
0xF9[7:0] = 0x00	► 4.2.9
Set up the video input mode	
0x15[3:0] – Video Format ID (default = 4:4:4)	►4.3.2
0x16[5:4] – Input Color Depth for 4:2:2 (default = 12 bit)	►4.3.2
0x16[3:2] – Video Input Style (default style = 2)	►4.3.2
0x17[1] – Aspect ratio of input video (4x3 = 0b0, 16x9 = 0b1)	►4.3.3
Set up the video output mode	
0x16[7:6] = 0b0 for 4:4:4 – Output Format (4:4:4 vs 4:2:2)	►4.3.5
0x18[7] = 0b1 for YCbCr to RGB – CSC Enable	►4.3.8
0x18[6:5] = 0b00 for YCbCr to RGB – CSC Scaling Factor	►4.3.8
0xAF[1] = 0b1 for HDMI – Manual HDMI or DVI mode select	► 4.2.2
0x40[7] = 0b1 – Enable GC	► 4.3.6
0x4C[3:0] – Output Color Depth and General Control Color Depth (GC CD)	► 4.3.6
HDCP	
0xAF[7] = 0b1 for enable HDCP	►4.7
0x97[6] – BKSV Interrupt Flag (Wait for value to be 0b1 then write 0b1)	►4.7
Audio setup	
0x01 – 0x03 = 0x001800 for 48kHz - N Value	►4.4.2
0x0A[6:4] – Audio Select (I2S = 0b000, SPDIF = 0b001, DSD = 0b010, HBR = 0b011, DST = 0b011)	► 4.4.1
Audio Mode	
0x0B[7] = 0b1 – SPDIF Enable	► 4.4.1.2
0x0C[5:2] = 0b1111 – I2S Enable	► 4.4.1.1
0x46 = 0xFF – DSD Enable	► 4.4.1.3
0x15[7:4] – I2S Sampling Frequency	► 4.4.1.1
0x0A[3:2] – Audio Mode	►4.4.1
0x0A[3:2] – Audio Select	► 4.4.1

SECTION 4 - PROGRAMMING TASKS

4.1 I2C Bus

The ADV7511 uses four I2C register maps. The SDA/SCL programming address for the Main Register Map is 0x72 or 0x7A, based on whether PD/AD is pulled high (10KΩ resistor to power supply = 0x7A) or pulled low (10KΩ resistor to GND = 0x72) when power is applied to the supplies. The user should wait 200ms for the address to be decided, after the power supplies are high, before attempting to communicate with the ADV7511 using I2C. A complete listing of the Main Register Map is provided in Section 5 -Register Maps Refer to the "I2C Interface (access to the ADV7511 registers)" section in the ▹ *ADV7511 Hardware User's Guide* for information about I2C hardware.

The device address for the Packet Memory is programmable and is controlled by register 0x45 of the Main Register Map. The default setting is 0x70. The details of the Packet Memory Map can be found in ► Table 112.

The EDID Memory address is programmable and controlled by register 0x43 of the Main Register Map.The default setting is 0x7E. The details of the CEC Memory Map can be found in ► Table 113.

The CEC Memory address is programmable and controlled by register 0xE1 of the Main Register Map. The default setting is 0x78. Unless otherwise stated, all register references in this document refer to the Main Register Map.

The Fixe I2C Address register 0xF9 needs to be set to an I2C address that does not conflict with any other address on the board. 0x00 is an appropriate setting.

Table 1 I2C Bus Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x43	R/W	[7:0]	01111110	EDID Memory Address	The I2C address for EDID memory
0x44	R/W	[0]	*******1	Packet Read Mode	Packet Memory Read Mode 0=Allow user to read from packet memory 1=Allow HDMI logic to read from packet memory
0x45	R/W	[7:0]	01110000	Packet Memory I2C Map Address	The I2C address for the packet memory
0xE1	R/W	[7:0]	01111000	CEC Map Address	The I2C address for CEC I2C control map
0xF9	R/W	[7:0]	01111100	Fixed I2C Address	This should be set to a non-conflicting I2C address (set to 0x00)

4.2 General Control

4.2.1 Hot Plug Detect (HPD) and Monitor Sense

To operate the ADV7511, it is necessary to monitor the Hot Plug Detect (HPD) signal and power up the part after HPD becomes high. To power up the part, the Power Down register bit (0x41[6]) must be written to 0 when the HPD pin is high. The status of the HPD pin can be read in register bit 0x42[6]. Both the HPD pin and Capability Discovery and Control (CDC) HPD will be used for the internal HDCP signal. The CDC HPD signal is used as the HPD signal when HEC is active, because the physical HPD line needs to be held high for HEC. The HPD source can be selected with the HPD Control Register Bits 0xD6[7:6]. When these bits are set to 0b00, both the HPD pin and CDC HPD will be used for the internal HPD signal. When these bits are set to0b01 only the CDC HPD will be used, and 0b10 means that only the HPD pin will be used. When 0xD6[7:6] is set to 0b11 the HPD signal will always be high, but the HPD interrupt will still respond to the HPD pin. To use the CDC HPD register bit 0x7F[6] of the CEC Map must be set to 1 and 0x80 and 0x81of the CEC Map need to be set to products containing the HDMI Tx's physical address.

When the signal on HPD is low, some registers cannot be written to. When HPD goes from high to low, some registers will be reset to their defaults. For additional details see ► Table 97. Refer to ► 4.11 for details on the use of interrupts.

If there is a need to power up the part when the HPD signal is low, the HPD can be overridden using the HPD Control register bit (0xD6[7] = 1. This would be needed, for example, when reading the EDID from an HDMI port when the HPD is low in order to find its CEC physical address.

The best method to determine when the HPD is high is to use the interrupt system. The bit representing an HPD interrupt is 0x96[7]. Refer to ► 4.11 for details on the use of interrupts.

Monitor Sense refers to the detection of TMDS clock line pull-ups in the HDMI sink. If greater than 1.8V is detected, the Monitor Sense interrupt will be triggered and the Monitor Sense State bit (0x42[5]) will be 1.

One reason to detect the Monitor Sense is to delay powering up the chip until the Rx is actually ready to receive signals. A typical implementation for a sink is to tie the HDMI 5V to HPD through a series resistor. In this case, the HPD signal will be detected regardless of whether the sink is powered on and ready to receive audio and video. For this reason it is best to wait for both the Monitor Sense and HPD before powering up the chip when trying to achieve minimum power consumption.

An internal weak pull-down resistor is available in the HDMI Tx to reduce BOM cost. This can be enabled by setting the HPD Pull Down register bit 0xE0[0] to 1.

Table 2 **Hot Plug Detect (HPD) and Monitor Sense Related Registers (Main Map)**

Address	Type	Bits	Default Value	Register Name	Function
0x42	RO	[6]	*0******	HPD State	State of HDMI sink 0 = Hot Plug Detect state is low 1 = Hot Plug Detect state is high
		[5]	**0*****	Monitor Sense State	State of the monitor connection 0 = HDMI clock termination not detected 1 = HDMI clock termination detected
0x94	R/W	[7]	1*******	HPD Interrupt Enable	HPD Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[6]	*1******	Monitor Sense Interrupt Enable	Monitor Sense Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x96	R/W	[7]	0*******	HPD Interrupt	HPD Interrupt 0 = no interrupt detected 1 = interrupt detected
		[6]	*0******	Monitor Sense Interrupt	Monitor Sense Interrupt 0 = no interrupt detected 1 = interrupt detected
0xA1	R/W	[6]	*0******	Monitor Sense Power Down	Monitor Sense Power Down 0 = Monitor Sense monitoring enabled 1 = Monitor Sense monitoring disabled
0xD6	R/W	[7:6]	00******	HPD Control	HPD Control 00 = HPD is from both HPD pin or CDC HPD 01 = HPD is from CDC HPD 10 = HPD is from HPD pin 11 = HPD is always high

Table 3 Hot Plug Detect (HPD) and Monitor Sense Related Registers (CEC Map)

Address	Type	Bits	Default Value	Register Name	Function
0x7F	R/W	[6]	*1******	CDC HPD Response Enable	Controls whether to toggle internal HPD signals when receiving CDC HPD message 1 = enable 0 = disable
0x80	R/W	[15:0]	00000000	CEC Physical Address	Physical address of CEC device
0x81			00000000		
0x82	R/W	[7:0]	00000001	CDC HPD Timer Count	Controls the time CDC HPD stays low when receiving CDC HPD toggle message. HPD low = CDC_HPD_Timer_Count * CEC_CLK. CEC_CLK is 760KHz by default.
0x83	RO	[7]	0*******	CDC HPD	HPD signal from CEC interface

4.2.2 HDMI DVI Selection

The HDMI Transmitter supports both HDMI and DVI modes. HDMI or DVI mode is selected by 0xAF[1]. In DVI mode no packets will be sent, and all registers relating to packets and InfoFrames will be disregarded. DVI only supports the RGB color space, so, if the input is not RGB, it is important to remember to set the color space conversion to output RGB when DVI is enabled. See ► 0 for details about the Color Space Converter. The current mode of HDMI or DVI can be confirmed by the read only (RO) bit 0xC6[4].

Table 4 HDMI DVI Selection Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0xAF	R/W	[1]	******0*	HDMI/DVI Mode Select	HDMI Mode 0 = DVI Mode 1 = HDMI Mode

4.2.3 AV Mute

The AV Mute bits are sent to the Rx through the General Control Packet (GCP). One purpose of the AV Mute is to alert the Rx of a change in the TMDS clock so the Rx can mute audio and video. AV Mute also pauses HDCP encryption, so the HDCP link is maintained while the TMDS clock is not stable. It can also be used in general to tell the sink to mute audio and video. AV Mute is not sufficient as a means to hide protected content, because the content is still sent even when AV Mute is enabled.

To use AV Mute, enable the GCP by setting the GC Packet Enable register bit (0x40[7]) to 1. To set AV mute, clear the Clear AV Mute bit (0x4B[7] = 0) and set the Set AV Mute bit (0x4B[6] = 1). To clear AV mute, clear Set AV Mute (0x4B[6] = 0) and set Clear AV Mute (0x4B[7] = 1). Note that it is invalid to set both bits to 1.

To avoid a partial update of the General Control packet, the Packet Update features should be used. By setting the GC Packet Update register bit (0x48[4] Packet Memory) to 1, the current values for GC Header and Packet Bytes will be stored and sent in the GC Packets. The user should update the values then set the GC Packet Update register bit to 0 to begin sending the new packets.

Table 5 AV Mute Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[7]	0*******	GC Packet Enable	GC Packet Enable 0 = GC Packet Disabled 1 = GC Packet Enabled
0x4A	R/W	[4]	***0****	GC Packet Update	GC Packet Update: Before updating the GC Packet using I2C set to '1' to continue sending the current values. 0 = GC Packet I2C update inactive 1 = GC Packet I2C update active
0x4B	R/W	[7]	0*******	Clear AV Mute	Clear Audio Video Mute 0 = Clear 1 = Set clear av mute
		[6]	*0******	Set AV Mute	Set Audio Video Mute 0 = Clear 1 = Set av mute.

4.2.4 TMDS Power-Down

The differential outputs of the ADV7511 can be powered down. This can be useful for ensuring that no invalid data will be put on the HDMI link until the register settings have been confirmed.

To avoid glitches in the TMDS clock at turn-on, a soft TMDS clock turn-on feature is provided. Enable the two Soft TMDS Clock Turn On registers before disabling Clock Driver Power Down. When the clock is active, disable the Soft TMDS Clock Turn On registers.

The TMDS Clock can be inverted by setting the TMDS Clock Inversion register bit 0xDE[3] to 1. This can be useful when using test equipments that has a dependency on the relationship between the TMDS clock and data.

Table 6 TMDS Power-Down Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0xA1	R/W	[5]	**0*****	Channel 0 Power Down	Channel 0 Power Down 0 = power up 1 = power down
		[4]	***0****	Channel 1 Power Down	Channel 1 Power Down 0 = power up 1 = power down
		[3]	****0***	Channel 2 Power Down	Channel 2 Power Down 0 = power up 1 = power down
		[2]	*****0**	Clock Driver Power Down	Clock Driver Power Down 0 = power up 1 = power down
0xD6	R/W	[4]	***0****	TMDS CLK Soft Turn On	Soft TMDS Clock Turn On 0 = Soft Turn On Disabled 1 = Soft Turn On Enabled
0xDE	R/W	[3]	****0***	TMDS Clock Inversion	TMDS Clock Inversion 0 = Normal TMDS Clock 1 = Inverted TMDS Clock

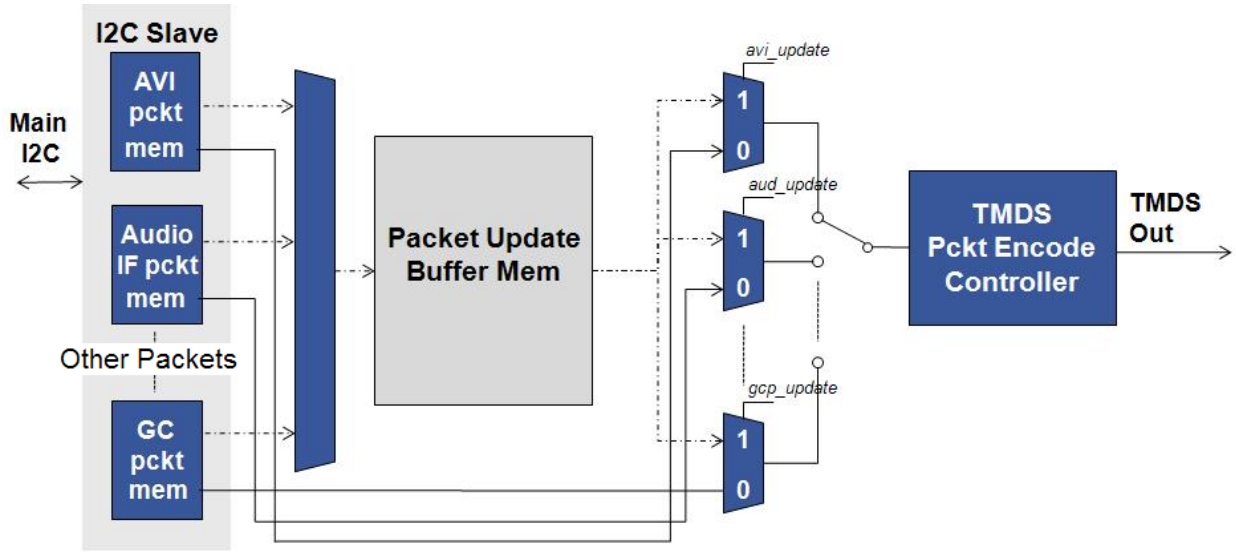
4.2.5 Packet Update

To avoid a partial update of the packets the Packet Update feature should be used. By setting the Packet Update register bit to 1the current values will be stored and sent in the packets. The user should update the values then set the Packet Update register bit to 0 to begin sending the new packets. The Packet Update feature is available for the following packets.

- AVI InfoFrame
- Audio InfoFrame
- GC Packet
- SPD Packet
- ACP Packet
- ISRC1 Packet
- ISRC2 Packet
- Spare Packet1
- Spare Packet2

►Figure 1 shows a block diagram depicting the internal structure of the Packet Update block of the ADV7511. As seen in ►Figure 1, only one Packet Update Buffer is available, which means that only one Packet can be updated at a given time. When the respective Packet Update register bit is set to '1', the contents of the packet are copied over from I2C memory to the Packet Update Buffer, and during this time the I2C contents can be updated without causing any disturbances on the screen. Copying over from I2C memory contents to the Packet Update Buffer happens within one TMDS clock cycle. Once the update is finished, the respective Packet Update register bit can set back to '0', and the next packet can be updated. As seen in the below figure, when the respective Packet Update register bit is set to '1', the contents of the Packet Update Buffer are used instead of the I2C memory contents to send across the TMDS link.It should be noted that at all packet updates are sent across the TMDS link during the next available blanking period.

Figure 1 **Packet Update**



4.2.6 Source Product Description (SPD) Packet

The Source Product Description (SPD) packet contains the vendor name and product description. One application of this packet is to allow the Rx to display the source information on an OSD. This information is in 7-bit ASCII format. Refer to the ▹ *HDMI 1.4* specification for more detail.

To avoid a partial update of the SPD packet the Packet Update features should be used. By setting the SPD Packet Update register bit (0x1F[7] Packet Memory) to 1, the current values for SPD Header and Packet Bytes (0x0 – 0x1E Packet Memory) will be stored and sent in the SPD packets. The user should update the values then set the SPD Packet Update register bit to '0' to begin sending the new packets. See section 4.2.5 for details.

Table 7 Source Product Description (SPD) Packet Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[6]	*0******	SPD Packet Enabled	SPD Packet Enable 0 = Disabled 1 = Enabled
0x4A	R/W	[7]	1*******	Auto Checksum Enable	Auto Checksum Enable 0 = Use checksum from registers 1 = Use automatically generated checksum

Table 8 Source Product Description (SPD) Packet Related Registers (Packetmemory Map)

Address	Type	Bits	Default Value	Register Name	Function
0x00	R/W	[7:0]	00000000	SPD Header Byte 0	
0x01	R/W	[7:0]	00000000	SPD Header Byte 1	
0x02	R/W	[7:0]	00000000	SPD Header Byte 2	
0x03	R/W	[7:0]	00000000	SPD Packet Byte 0	
…	…	…	…	…	…
0x1E	R/W	[7:0]	00000000	SPD Packet Byte 27	
0x1F	R/W	[7]	0*******	SPD Packet Update	SPD Packet Update: Before updating the SPD Packet using I2C set to '1' to continue sending the current values. 0 = SPD Packet I2C update inactive 1 = SPD Packet I2C update active

4.2.7 Spare Packets

Spare packets are defined by the user. This allows the ADV7511 to adapt to future changes and additions to the ▹ HDMI specification.

To avoid a partial update of the Spare Packets the Packet Update features should be used. By setting the Spare Packet 1 Update register bit (0xDF[7] Packet Memory) or Spare Packet 2 Update register bit (0xFF[7] Packet Memory) to 1, the current values will be stored in the Spare Packet Header and Packet Bytes (0xC0 – 0xDE and 0xE0 to 0xFE Packet Memory) and sent in the Spare Packets. The user should update the values then set the Spare Packet 1 Update or Spare Packet 2 Update register bit to '0' to begin sending the new packets. See section 4.2.5 for details.

Table 9 Spare Packets Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[1]	******0*	Spare Packet 2 Enable	Spare Packet 2 Enable 0 = Disabled 1 = Enabled
		[0]	*******0	Spare Packet 1 Enable	Spare Packet 1 Enable 0 = Disabled 1 = Enabled

Table 10 Spare Packets Related Registers (Packetmemory Map)

Address	Type	Bits	Default Value	Register Name	Function
0xC0	R/W	[7:0]	00000000	Spare Packet 1 Header Byte 0	
0xC1	R/W	[7:0]	00000000	Spare Packet 1 Header Byte 1	
0xC2	R/W	[7:0]	00000000	Spare Packet 1 Header Byte 2	
0xC3	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 0	
…	…	…	…	…	…
0xDE	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 27	
0xDF	R/W	[7]	0*******	Spare Packet 1 Update	Spare Packet 1 Update Before updating the Spare Packet1 using I2C set to '1' to continue sending the current values. 0 = Spare Packet 1 I2C update inactive. 1 = Spare Packet 1 I2C update active.
0xE0	R/W	[7:0]	00000000	Spare Packet 2 Header Byte 0	
…	…	…	…	…	…
0xFE	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 27	
0xFF	R/W	[7]	0*******	Spare Packet 2 Update	Spare Packet 2 Update Before updating the Spare Packet 2 using I2C set to '1' to continue sending the current values. 0 = Spare Packet 2 I2C update inactive 1 = Spare Packet 2 I2C update active

4.2.8 System Monitoring

The ADV7511 utilizes both interrupts and registers to report errors and the status of internal operations. See ► 4.11 for details about using interrupts.

4.2.8.1 DDCController Status

The current state of the DDC controller can be read from the DDC Controller State I2C register (0xC8 [3:0]). The codes for this register are shown in ► Table 11.

Table 11 DDCController Status

0xC8 [3:0]	DDC ControllerState
0000	In Reset (No Hot Plug Detected)
0001	Reading EDID
0010	IDLE (Waiting for HDCP Requested)
0011	Initializing HDCP
0100	HDCP Enabled
0101	Initializing HDCP Repeater

4.2.8.2 HDCP/EDID Controller Error Codes

If an error occurs, the ADV7511 can send and interrupt. See ► 4.11 for details about using interrupts. An error code is then reported in the DDC Controller Error register (0xC8 [7:4]). ► Table 12 lists the possible error conditions and the corresponding 4-bit error code. The error code is only valid when the error interrupt is 1. The last error code will remain in the DDC Controller Error register even when the interrupt is cleared.

Table 12 Error Code Definitions

Error Code	Error Condition
0000	No Error
0001	Bad Receiver BKSV
0010	Ri Mismatch
0011	Pj Mismatch
0100	I2C Error (usually a no-ack)
0101	Timed Out Waiting for Downstream Repeater DONE
0110	Max Cascade of Repeaters Exceeded
0111	SHA-1 Hash Check of KSV List Failed
1000	Too Many Devices Connected to Repeater Tree

Table 13 System Monitoring Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x95	R/W	[7]	0*******	DDC Controller Error Interrupt Enable	DDC Controller Error Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x97	R/W	[7]	0*******	DDC Controller Error Interrupt	DDC Controller Error Interrupt 0 = no interrupt detected 1 = interrupt detected
0x9E	RO	[4]	***0****	PLL Lock Status	PLL Lock Status 0 = PLL Not Locked 1 = PLL Locked
0xC8	RO	[7:4]	0000****	DDC Controller Error	DDC Controller Error Error code report when the DDC Controller Error Interrupt register 0x97[7] = 1
		[3:0]	****0000	DDC Controller State	DDC Controller State State of the controller used for HDCP debug purposes

4.2.9 Fixed Registers That Must Be Set

After HPD becomes low the ADV7511 will be powered down and many registers reset. When HPD becomes high, it must be powered up by using the Power Down register bit (0x41[6]). The following fixed registers should be set after power up:

Table 14 Fixed Registers That Must Be Set (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x98	R/W	[7:0]	00001011	Fixed	Must be set to0x03 for proper operation
0x9A	R/W	[7:1]	0000000*	Fixed	Must be set to 0b1110000
0x9C	R/W	[7:0]	01011010	Fixed	Must be set to 0x30 for proper operation
0x9D	R/W	[1:0]	******00	Fixed	Must be set to 0b01 for proper operation
0xA2	R/W	[7:0]	10000000	Fixed	Must be set to 0xA4 for proper operation
0xA3	R/W	[7:0]	10000000	Fixed	Must be set to 0xA4 for proper operation
0xE0	R/W	[7:0]	10000000	Fixed	Must be set to 0xD0 for proper operation
0xF9	R/W	[7:0]	01111100	Fixed I2C Address	This should be set to a non-conflicting I2C address (set to 0x00)

4.3 Video Setup

4.3.1 Input Formatting

The ADV7511 accepts video data from as few as eight pins (either YCbCr 4:2:2 double data rate [DDR] or YCbCr 4:2:2 with 2x pixel clock) or as many as 36 pins (RGB 4:4:4 or YCbCr 4:4:4). In addition it accepts HSYNC, VSYNC and DE (Data Enable). The ADV7511 is able to detect all of the 59 video formats defined in the ▹ *EIA/CEA-861D* specification. Either

separate HSYNC, VSYNC, and DE, or embedded syncs in the style of the ITU BT.656, SMPTE 274M, and SMPTE 296M specifications are accepted. If less than 36 input pins are used, the alignment of the data can be defined as left justified (all data begins from D35), right justified (all data ends at D0), or evenly distributed. In the case of evenly distributed, the channel data is left-justified in their respective 12-bit fields. For example, an evenly distributed 24-bit RGB signal would have R[7:0] mapped to D[35:28]; G[7:0] mapped to D[23:16]; and B[7:0] mapped to D[11:4].

- ▹ For timing details for video capture, refer to the *Functional Description* section of the *ADV7511 Hardware User Guide*.

The tables in ► 4.3.2 define how the many different formats are accepted on the input data lines.

4.3.2 Video Input Tables

Table 15 Input ID Selection

Input ID	Bits per Color	Pin Assignment Table	Maximum Input Clock	Format Name	Sync Type
0	8, 10	Table 16	165.0 MHz	RGB 4:4:4, YCbCr 4:4:4	Separate syncs
	12	Table 16	150.0 MHz	RGB 4:4:4, YCbCr 4:4:4	Separate syncs
1	8, 10, 12	Table 17 – Table 19	165.0 MHz	YCbCr 4:2:2	Separate syncs
2	8, 10, 12		165.0 MHz	YCbCr 4:2:2	Embedded syncs
3	8, 10, 12	Table 20 – Table 22	82.5 MHz	YCbCr 4:2:2 2X clock	Separate syncs
4	8, 10, 12		82.5 MHz	YCbCr 4:2:2 2X clock	Embedded syncs
5	8, 10, 12	Table 23 – Table 24	82.5 MHz	RGB 4:4:4, YCbCr 4:4:4 DDR	Separate syncs
6	8, 10, 12	Table 25 – Table 27	82.5 MHz	YCbCr 4:2:2 DDR	Separate syncs
7	8, 10, 12	Table 20 – Table 22	82.5 MHz	YCbCr 4:2:2 DDR	Separate syncs
8	8, 10, 12		82.5 MHz	YCbCr 4:2:2 DDR	Embedded syncs

Table 16 Normal RGB or YCbCr 4:4:4 (36, 30, or 24 bits) with Separate Syncs; Input ID = 0

Mode	Format	Input Data D[35:0]																																	
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
36 bit	RGB	R[11:0]												G[11:0]												B[11:0]											
	YCrCb	Cr[11:0]												Y[11:0]												Cb[11:0]											
30 bit	RGB	R[9:0]												G[9:0]												B[9:0]											
	YCrCb	Cr[9:0]												Y[9:0]												Cb[9:0]											
24 bit	RGB	R[7:0]												G[7:0]												B[7:0]											
	YCrCb	Cr[7:0]												Y[7:0]												Cb[7:0]											
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

An input format of RGB 4:4:4 or YCbCr 4:4:4 can be selected by setting the input ID (0x15 [3:0]) to 0x0. There is no need to set the Input Style (0x16[3:2]) or channel alignment (0x48[4:3]). For timing details see the ▹ *ADV7511 Hardware User's Guide*.

Table 17 YCbCr 4:2:2 Formats (24, 20, or 16 bits) Input Data Mapping: 0x48[4:3] = '10' (left justified) Input ID = 1 or 2

Mode	Pixel	Input Data D[35:0]																																							
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
		Style 1																																							
24 bit	1st	Cb[11:4]								Y[11:4]								Cb[3:0]				Y[3:0]																			
	2nd	Cr[11:4]								Y[11:4]								Cr[3:0]				Y[3:0]																			
20 bit	1st	Cb[9:2]								Y[9:2]								Cb [1:0]				Y [1:0]																			
	2nd	Cr[9:2]								Y[9:2]								Cr [1:0]				Y [1:0]																			
16 bit	1st	Cb[7:0]								Y[7:0]																															
	2nd	Cr[7:0]								Y[7:0]																															
		Style 2																																							
24bit	1st	Cb[11:0]												Y[11:0]																											
	2nd	Cr[11:0]												Y[11:0]																											
20 bit	1st	Cb[9:0]										Y[9:0]																													
	2nd	Cr[9:0]										Y[9:0]																													
16 bit	1st	Cb[7:0]								Y[7:0]																															
	2nd	Cr[7:0]								Y[7:0]																															
		Style 3																																							
24 bit	1st	Y[11:0]												Cb[11:0]																											
	2nd	Y[11:0]												Cr[11:0]																											
20 bit	1st	Y[9:0]										Cb[9:0]																													
	2nd	Y[9:0]										Cr[9:0]																													
16 bit	1st	Y[7:0]								Cb[7:0]																															
	2nd	Y[7:0]								Cr[7:0]																															
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID = 1: An input with **YCbCr 4:2:2 with separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0001. The data bit width (24, 20, or 16 bits) must be set with 0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2].

Input ID = 2: An input with **YCbCr 4:2:2 with embedded syncs** (SAV [Start of Active Video] and EAV [End of Active Video]) can be selected by setting the Input ID (0x15[3:0]) to 0b0010. The data bit width (24 = 12 bits, 20 = 10 bits, or 16 = 8 bits) must be set with 0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.

Table 18 YCbCr 4:2:2 Formats (24, 20, or 16 bits) Input Data Mapping: 0x48[4:3] = '01' (right justified) Input ID = 1 or 2

Mode	Pixel	Input Data D[35:0]																																							
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
		Style 1																																							
24 bit	1st													Cb[11:4]								Y[11:4]								Cb[3:0]				Y[3:0]						
	2nd													Cr[11:4]								Y[11:4]								Cr[3:0]				Y[3:0]						
20 bit	1st													Cb[9:2]								Y[9:2]								Cb [1:0]				Y [1:0]						
	2nd													Cr[9:2]								Y[9:2]								Cr [1:0]				Y [1:0]						
16 bit	1st													Cb[7:0]								Y[7:0]																			
	2nd													Cr[7:0]								Y[7:0]																			
		Style 2																																							
24 bit	1st													Cb[11:0]												Y[11:0]															
	2nd													Cr[11:0]												Y[11:0]															
20 bit	1st													Cb[9:0]										Y[9:0]																	
	2nd													Cr[9:0]										Y[9:0]																	
16 bit	1st													Y[7:0]								Cb[7:0]																			
	2nd													Y[7:0]								Cr[7:0]																			
		Style 3																																							
24 bit	1st													Y[11:0]												Cb[11:0]															
	2nd													Y[11:0]												Cr[11:0]															
20 bit	1st													Y[9:0]										Cb[9:0]																	
	2nd													Y[9:0]										Cr[9:0]																	
16 bit	1st													Y[7:0]								Cb[7:0]																			
	2nd													Y[7:0]								Cr[7:0]																			
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID = 1: An input with **YCbCr 4:2:2 with separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0001. The data bit width (24, 20, or 16 bits) must be set with 0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2].

Input ID = 2: An input with **YCbCr 4:2:2 with embedded syncs** (SAV and EAV) can be selected by setting the Input ID (0x15[3:0]) to 0b0010. The data bit width (24 = 12 bits, 20 = 10 bits, or 16 = 8 bits) must be set with 0x16 [5:4]. The threeinput pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.

Table 19 YCbCr 4:2:2 Formats (24, 20, or 16 bits) Input Data Mapping: 0x48[4:3] = '00' (evenly distributed) Input ID = 1 or 2

Mode	Pixel	Input Data D[35:0]																																					
		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
		Style 1																																					
24 bit	1st	Cb[11:4]												Y[11:4]												Cb[3:0]				Y[3:0]									
	2nd	Cr[11:4]												Y[11:4]												Cr[3:0]				Y[3:0]									
20 bit	1st	Cb[9:2]												Y[9:2]												Cb [1:0]				Y [1:0]									
	2nd	Cr[9:2]												Y[9:2]												Cr [1:0]				Y [1:0]									
16 bit	1st	Cb[7:0]												Y[7:0]																									
	2nd	Cr[7:0]												Y[7:0]																									
		Style 2																																					
24 bit	1st	Cb[11:4]												Cb[3:0]				Y[11:8]								Y[7:0]													
	2nd	Cr[11:4]												Cr[3:0]				Y[11:8]								Y[7:0]													
20 bit	1st	Cb[9:2]												Cb [1:0]		Y[9:4]										Y[3:0]													
	2nd	Cr[9:2]												Cr [1:0]		Y[9:4]										Y[3:0]													
16 bit	1st	Cb[7:0]												Y[7:0]																									
	2nd	Cr[7:0]												Y[7:0]																									
		Style 3																																					
24 bit	1st	Y[11:4]												Y[3:0]				Cb[11:8]								Cb[7:0]													
	2nd	Y[11:4]												Y[3:0]				Cr[11:8]								Cr[7:0]													
20 bit	1st	Y[9:2]												Y [1:0]		Cb[9:4]										Cb[3:0]													
	2nd	Y[9:2]												Y [10]		Cr[9:4]										Cr[3:0]													
16 bit	1st	Y[7:0]												Cb[7:0]																									
	2nd	Y[7:0]												Cr[7:0]																									
Pins D[35:0]		35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID = 1: An input with **YCbCr 4:2:2 with separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0001. The data bit width (24, 20, or 16 bits) must be set with 0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2].

Input ID = 2: An input with **YCbCr 4:2:2 with embedded syncs** (SAV and EAV) can be selected by setting the Input ID (0x15[3:0]) to 0b0010. The data bit width (24 = 12 bits, 20 = 10 bits, or 16 = 8 bits) must be set with 0x16 [5:4]. The three input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like an ITU 656 style bus running at 1X clock and double width.

Table 20 YCbCr 4:2:2 Formats (12,10, or 8 bits) Input Data Mapping: 0x48[4:3]=10(left justified) Input ID=3,4,7or 8

Mode	Pixel	Edge	Input Data D[35:0]																																															
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00													
Style 1																																																			
12 bit	1	1									Cb[11:4]												Cb[3:0]																													
		2									Y[11:4]												Y[3:0]																													
	2	1									Cr[11:4]												Cb[3:0]																													
		2									Y[11:4]												Y[3:0]																													
10 bit	1	1									Cb[9:2]												Cb [1:0]																													
		2									Y[9:2]												Y [1:0]																													
	2	1									Cr[9:2]												Cr [1:0]																													
		2									Y[9:2]												Y [1:0]																													
8 bit	1	1									Cb[7:0]																																										
		2									Y[7:0]																																											
	2	1									Cr[7:0]																																										
		2									Y[7:0]																																											
Style 2																																																			
12 bit	1	1													Cb[11:0]																																					
		2													Y[11:0]																																					
	2	1													Cr[11:0]																																					
		2													Y[11:0]																																					
10 bit	1	1															Cb[9:0]																																				
		2															Y[9:0]																																				
	2	1															Cr[9:0]																																				
		2															Y[9:0]																																				
8 bit	1	1																Cb[7:0]																																				
		2																Y[7:0]																																				
	2	1																Cr[7:0]																																				
		2																Y[7:0]																																				
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00													

Input ID = 3: An input with **YCbCr 4:2:2 data and separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0011. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate**. For timing details, see the ▹ *ADV7511 Hardware User's Guide* and► Figure 2.

Input ID = 4: An input with **YCbCr 4:2:2 and embedded syncs** (ITU 656 based) can be selected by setting the Input ID (0x15[3:0]) to 0b0100. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The order of data input is the order in the table. For example, data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3… Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate.** For timing details, see the ▹ *ADV7511 Hardware User's Guide* and► Figure 2.

Input ID=7: A DDR input with **YCbCr 4:2:2 data and separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0111. The This input format is the same as input ID 3 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR). For timing details, see the ▹ *ADV7511 Hardware User's Guide and* ►Figure 3 and ► Figure 4. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

Input ID=8: A DDR input with **YCbCr 4:2:2 and embedded syncs** (ITU656-based) can be selected by setting Input ID (0x15[3:0]) to 0b1000. This input format is the same as input ID 4 except that the clock is not 2X the pixel rate, but is double data rate (DDR). For timing details, see the ▹ *ADV7511 Hardware User's Guide and* ►Figure 3 and ► Figure 4. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

Table 21 YCbCr 4:2:2 Formats (12,10 or 8 bits) Input Data Mapping: 0x48[4:3]=01(right justified) Input ID=3,4,7 or 8

Mode	Pixel	Edge	Input Data D[35:0]																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
			Style 1																																					
12 bit	1	1																					Cb [11:4]												[3:0]			
		2																					Y[11:4]												[3:0]			
	2	1																					Cr [11:4]												[3:0]			
		2																					Y[11:4]												[3:0]			
10 bit	1	1																					Cb [9:2]												[1:0]			
		2																					Y[9:2]												[1:0]			
	2	1																					Cr [9:2]												[1:0]			
		2																					Y[9:2]												[1:0]			
8 bit	1	1																					Cb [7:0]															
		2																					Y[7:0]															
	2	1																					Cr [7:0]															
		2																					Y[7:0]															
			Style 2																																					
12 bit	1	1																									Cb [11:0]											
		2																									Y[11:0]											
	2	1																									Cr [11:0]											
		2																									Y[11:0]											
10 bit	1	1																											Cb [9:0]									
		2																											Y[9:0]									
	2	1																											Cr [9:0]									
		2																											Y[9:0]									
8 bit	1	1																													Cb [7:0]							
		2																													Y[7:0]							
	2	1																													Cr [7:0]							
		2																													Y[7:0]							
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID = 3: An input with **YCbCr 4:2:2 data and separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0011. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate**. For timing details, see the ▹ *ADV7511 Hardware User's Guide* and► Figure 2.

Input ID = 4: An input with **YCbCr 4:2:2 and embedded syncs** (ITU 656 based) can be selected by setting the Input ID (0x15[3:0]) to 0b0100. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The order of data input is the order in the table. For example, data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3… Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate.** For timing details, see the ▹ *ADV7511 Hardware User's Guide* and► Figure 2.

Input ID=7: A DDR input with **YCbCr 4:2:2 data and separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0111. This input format is the same as input ID 3 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR). For timing details, see the ▹ *ADV7511 Hardware User's Guide and* ►Figure 3 and ► Figure 4. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

Input ID=8: A DDR input with **YCbCr 4:2:2 and embedded syncs** (ITU 656 based) can be selected by setting the Input ID (0x15[3:0]) to 0b1000. This input format is the same as input ID 4 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR). For timing details, see the ▹ *ADV7511 Hardware User's Guide and* ►Figure 3 and ► Figure 4. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

Table 22 YCbCr 4:2:2 Formats (12,10 or 8 bits) Input Data Mapping: 0x48[4:3]=00 (evenly dist.) Input ID=3,4,7 or 8

Mode	Pixel	Edge	Input Data D[35:0]																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Style 1																																						
12 bit	1	1													Cb [11:4]																[3:0]							
		2													Y[11:4]																[3:0]							
	2	1													Cr[11:4]																[3:0]							
		2													Y[11:4]																[3:0]							
10 bit	1	1													Cb [9:2]																[1:0]							
		2													Y[9:2]																[1:0]							
	2	1													Cr[9:2]																[1:0]							
		2													Y[9:2]																[1:0]							
8 bit	1	1													Cb [7:0]																							
		2													Y[7:0]																							
	2	1													Cr[7:0]																							
		2													Y[7:0]																							
Style 2																																						
12 bit	1	1																	Cb [11:8]								Cb [7:0]											
		2																	Y[11:8]								Y[7:0]											
	2	1																	Cr[11:8]								Cr[7:0]											
		2																	Y[11:8]								Y[7:0]											
10 bit	1	1																			Cb [9:8]						Cb [7:0]											
		2																			Y [9:8]						Y[7:0]											
	2	1																			Cr [9:8]						Cr[7:0]											
		2																			Y [9:8]						Y[7:0]											
8 bit	1	1																									Cb [7:0]											
		2																									Y[7:0]											
	2	1																									Cr[7:0]											
		2																									Y[7:0]											
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID = 3: An input with **YCbCr 4:2:2 data and separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0011. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate**. For timing details, see the ▹ *ADV7511 Hardware User's Guide* and▸ Figure 2.

Input ID = 4: An input with **YCbCr 4:2:2 and embedded syncs** (ITU 656 based) can be selected by setting the Input ID (0x15[3:0]) to 0b0100. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The two input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The order of data input is the order in the table. For example, data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3… Pixel 1 is the first pixel of the 4:2:2 word and should be where DE starts. **This mode requires an input clock 2X the pixel rate.** For timing details, see the ▹ *ADV7511 Hardware User's Guide* and▸ Figure 2.

Input ID=7: A DDR input with **YCbCr 4:2:2 data and separate syncs** can be selected by setting the Input ID (0x15[3:0]) to 0b0111. This input format is the same as input ID 3 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR). For timing details, see the ▹ *ADV7511 Hardware User's Guide and* ▸Figure 3 and ▸ Figure 4. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

Input ID=8: A DDR input with **YCbCr 4:2:2 and embedded syncs** (ITU656-based) is selected by setting the Input ID (0x15[3:0]) to 0b1000. This input format is the same as input ID 4 with the exception that the clock is not 2X the pixel rate, but is double data rate (DDR). For timing details, see the ▹ *ADV7511 Hardware User's Guide and* ▸Figure 3 and ▸ Figure 4. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge.

Figure 2 **2X Clock timing**

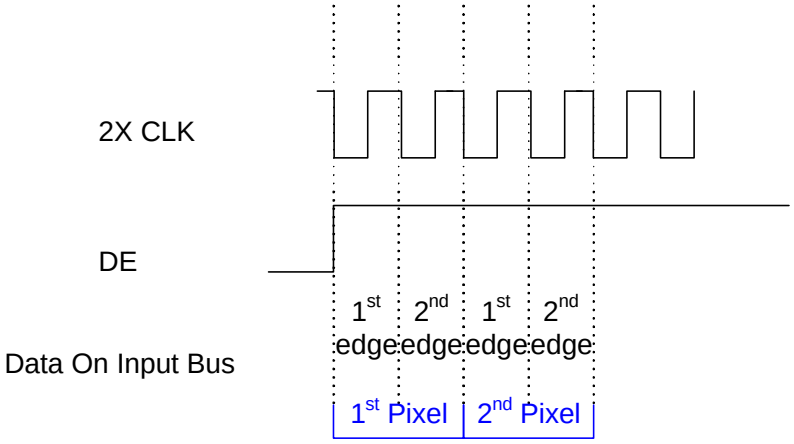


Table 23 RGB or YCbCr 4:4:4 (12 bits) DDR with Separate Syncs: Input ID = 5, left aligned (0x48[5] = 1)

Mode	Pixel	Edge	Input Data Mapping Input ID = 5																																					
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
			Style 1																																					
	1	1	G[5:0]												B[11:0]																									
		2	R[11:0]																		G[11:6]																			
	1	1	Y[5:0]												Cb[9:0]																									
		2	Cr[11:0]																		Y[11:6]																			
	1	1	G[4:0]					B[9:0]																																
		2	R[9:0]									G[9:5]																												
	1	1	Y[4:0]					Cb[9:0]																																
		2	Cr[9:0]									Y[9:5]																												
444	1	1	G[3:0]				B[7:0]																																
444		2	R[7:0]							G[7:4]																														
	1	1	Y[3:0]				Cb[7:0]																																
		2	Cr[7:0]							Y[7:4]																														
			Style 2																																					
	1	1	R[11:0]												G[11:6]																									
		2	G[4:0]												B[11:0]																									
	1	1	Cr[11:0]																		Y[11:6]																			
		2	Y[5:0]												Cb[11:0]																									
	1	1	R[9:0]									G[9:5]																												
		2	G[4:0]					B[9:0]																																
	1	1	Cr[9:0]									Y[9:5]																												
		2	Y[4:0]					Cb[9:0]																																
444	1	1	R[7:0]							G[7:4]																														
444		2	G[3:0]				B[7:0]																																
	1	1	Cr[7:0]							Y[7:4]																														
		2	Y[3:0]				Cb[7:0]																																
			Style 3																																					
	1	1	Y[11:0]												Cb[11:6]																									
		2	Cb[5:0]												Cr[11:0]																									
	1	1	Y[9:0]												Cb[9:5]																									
		2	Cb[4:0]					Cr[9:0]																																
444	1	1	Y[7:0]												Cb[7:4]																									
		2	Cb[3:0]					Cr[7:0]																																
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID=5: An input format of **RGB 4:4:4 DDR or YCbCr 4:4:4 DDR** can be selected by setting the input ID (0x15 [3:0]) to 0x5. The three input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

Table 24 RGB or YCbCr 4:4:4 (12 bits) DDR with Separate Syncs: Input ID = 5, right aligned (0x48[5] = 0)

Mode	Pixel	Edge	Input Data Mapping Input ID = 5																																			
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
			Style 1																																			
	1	1																			G[5:0]						B[11:0]											
		2																			R[11:0]												G[11:6]					
	1	1																			Y[5:0]						Cb[9:0]											
		2																			Cr[11:0]												Y[11:6]					
	1	1																						G[4:0]					B[9:0]									
		2																						R[9:0]										G[9:5]				
	1	1																						Y[4:0]					Cb[9:0]									
		2																						Cr[9:0]										Y[9:5]				
444	1	1																									G[3:0]				B[7:0]							
444		2																									R[7:0]								G[7:4]			
	1	1																									Y[3:0]				Cb[7:0]							
		2																									Cr[7:0]								Y[7:4]			
			Style 2																																			
	1	1																			R[11:0]												G[11:6]					
		2																			G[4:0]						B[11:0]											
	1	1																			Cr[11:0]												Y[11:6]					
		2																			Y[5:0]						Cb[11:0]											
	1	1																						R[9:0]										G[9:5]				
		2																						G[4:0]					B[9:0]									
	1	1																						Cr[9:0]										Y[9:5]				
		2																						Y[4:0]					Cb[9:0]									
444	1	1																									R[7:0]								G[7:4]			
444		2																									G[3:0]				B[7:0]							
	1	1																									Cr[7:0]								Y[7:4]			
		2																									Y[3:0]				Cb[7:0]							
			Style 3																																			
	1	1																			Y[11:0]												Cb[11:6]					
		2																			Cb[5:0]						Cr[11:0]											
	1	1																						Y[9:0]										Cb[9:5]				
		2																						Cb[4:0]					Cr[9:0]									
444	1	1																									Y[7:0]								Cb[7:4]			
		2																									Cb[3:0]				Cr[7:0]							
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Input ID=5: An input format of **RGB 4:4:4 DDR or YCbCr 4:4:4 DDR** can be selected by setting the input ID (0x15 [3:0]) to 0x5. The three input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

Table 25 YCbCr 4:2:2 (12, 10, or 8 bits) DDR with Separate Syncs: Input ID = 6, right justified (0x48[4:3] = '01')

Mode	Pixel	Edge	Input Data Mapping Input ID = 6																																														
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00											
YCbCr			Style 1																																															
12bit	1	1																									Y[7:4]				Cb[3:0]				Y[3:0]														
		2																									Cb[11:4]								Y[11:8]														
	2	1																									Y[7:4]				Cr[3:0]				Y[3:0]														
		2																									Cr[11:4]								Y[11:8]														
10bit	1	1																									Y[5:4]		Cb[3:0]				Y[3:0]																
		2																									Cb[9:4]						Y[9:6]																
	2	1																									Y[5:4]		Cr[3:0]				Y[3:0]																
		2																									Cr[9:4]						Y[9:6]																
8bit	1	1																									Cb[3:0]				Y[3:0]																		
		2																									Cb[7:4]				Y[7:4]																		
	2	1																									Cr[3:0]				Y[3:0]																		
		2																									Cr[7:4]				Y[7:4]																		
			Style 2																																															
12bit	1	1																									Y[11:0]																						
		2																									Cb[11:0]																						
	2	1																									Y[11:0]																						
		2																									Cr[11:0]																						
10bit	1	1																									Y[9:0]																						
		2																									Cb[9:0]																						
	2	1																									Y[9:0]																						
		2																									Cr[9:0]																						
8bit	1	1																									Y[7:0]																						
		2																									Cb[7:0]																						
	2	1																									Y[7:0]																						
		2																									Cr[7:0]																						
			Style 3																																															
12bit	1	1																									Cb[11:0]																						
		2																									Y[11:0]																						
	2	1																									Cr[11:0]																						
		2																									Y[11:0]																						
10bit	1	1																									Cb[9:0]																						
		2																									Y[9:0]																						
	2	1																									Cr[9:0]																						
		2																									Y[9:0]																						
8bit	1	1																									Cb[7:0]																						
		2																									Y[7:0]																						
	2	1																									Cr[7:0]																						
		2																									Y[7:0]																						
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00											

An input format of YCbCr 4:2:2 DDR can be selected by setting the input ID (0x15 [3:0]) to 0x6. The three different input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The Data Input Edge is defined in 0x16 [1]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

Table 26 YCbCr 4:2:2 (12, 10, or 8 bits) DDR with Separate Syncs: Input ID = 6, left justified (0x48[4:3] = '10')

Mode	Pixel	Edge	Input Data Mapping Input ID = 6																																					
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
YCbCr			Style 1																																					
12bit	1	1													Y[7:4]				Cb[3:0]				Y[3:0]																	
		2													Cb[11:4]								Y[11:8]																	
	2	1													Y[7:4]				Cr[3:0]				Y[3:0]																	
		2													Cr[11:4]								Y[11:8]																	
10bit	1	1													Y[5:4]		Cb[3:0]				Y[3:0]																			
		2													Cb[9:4]						Y[9:6]																			
	2	1													Y[5:4]		Cr[3:0]				Y[3:0]																			
		2													Cr[9:4]						Y[9:6]																			
8bit	1	1													Cb[3:0]				Y[3:0]																					
		2													Cb[7:4]				Y[7:4]																					
	2	1													Cr[3:0]				Y[3:0]																					
		2													Cr[7:4]				Y[7:4]																					
			Style 2																																					
12bit	1	1													Y[11:0]																									
		2													Cb[11:0]																									
	2	1													Y[11:0]																									
		2													Cr[11:0]																									
10bit	1	1													Y[9:0]																									
		2													Cb[9:0]																									
	2	1													Y[9:0]																									
		2													Cr[9:0]																									
8bit	1	1													Y[7:0]																									
		2													Cb[7:0]																									
	2	1													Y[7:0]																									
		2													Cr[7:0]																									
			Style 3																																					
12bit	1	1													Cb[11:0]																									
		2													Y[11:0]																									
	2	1													Cr[11:0]																									
		2													Y[11:0]																									
10bit	1	1													Cb[9:0]																									
		2													Y[9:0]																									
	2	1													Cr[9:0]																									
		2													Y[9:0]																									
8bit	1	1													Cb[7:0]																									
		2													Y[7:0]																									
	2	1													Cr[7:0]																									
		2													Y[7:0]																									
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

An input format of YCbCr 4:2:2 DDR can be selected by setting the input ID (0x15 [3:0]) to 0x6. The three different input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The Data Input Edge is defined in 0x16 [1]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

Table 27 YCbCr 4:2:2 (12, 10, or 8 bits) DDR with Separate Syncs: Input ID = 6, evenly distributed (0x48[4:3] = '00')

Mode	Pixel	Edge	Input Data Mapping Input ID = 6																																					
			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
YCbCr			Style 1																																					
12bit	1	1	Y[7:4]												Cb[3:0]												Y[3:0]											
		2	Cb[11:8]												Cb[7:4]												Y[11:8]											
	2	1	Y[7:4]												Cr[3:0]												Y[3:0]											
		2	Cr[11:8]												Cr[7:4]												Y[11:8]											
10bit	1	1	Y[5:4]		Cb[3:2]										Cb[1:0]		Y[3:2]										Y[1:0]											
		2	Cb[9:6]												Cb[5:4]		Y[9:8]										Y[7:6]											
	2	1	Y [5:4]		Cr [3:2]										Cr[1:0]		Y[3:2]										Y[1:0]											
		2	Cr[9:6]												Cr[5:4]		Y[9:6]										Y[5:4]											
8bit	1	1	Cb[3:0]												Y[3:0]																							
		2	Cb[7:4]												Y[7:4]																							
	2	1	Cr[3:0]												Y[3:0]																							
		2	Cr[7:4]												Y[7:4]																							
			Style 2																																					
12bit	1	1	Y[11:8]												Y[7:4]												Y[3:0]											
		2	Cb[11:8]												Cb[7:4]												Cb[3:0]											
	2	1	Y[11:8]												Y[7:4]												Y[3:0]											
		2	Cr[11:8]												Cr[7:4]												Cr[3:0]											
10bit	1	1	Y[9:6]												Y[5:2]												Y[1:0]											
		2	Cb[9:6]												Cb[5:2]												Cb[1:0]											
	2	1	Y[9:6]												Y[5:2]												Y[1:0]											
		2	Cr[9:6]												Cr[5:2]												Cr[1:0]											
8bit	1	1	Y[7:0]												Y[7:0]																							
		2	Cb[7:0]												Cb[7:0]																							
	2	1	Y[7:0]												Y[7:0]																							
		2	Cr[7:0]												Cr[7:0]																							
			Style 3																																					
12bit	1	1	Cb[11:8]												Cb[7:4]												Cb[3:0]											
		2	Y[11:0]												Y[7:4]												Y[3:0]											
	2	1	Cr[11:0]												Cr[7:4]												Cr[3:0]											
		2	Y[11:0]												Y[7:4]												Y[3:0]											
10bit	1	1	Cb[9:6]												Cb[5:2]												Cb[1:0]											
		2	Y[9:6]												Y[5:2]												Y[1:0]											
	2	1	Cr[9:6]												Cr[5:2]												Cr[1:0]											
		2	Y[9:6]												Y[5:2]												Y[1:0]											
8bit	1	1	Cb[7:4]												Cb[3:0]																							
		2	Y[7:4]												Y[3:0]																							
	2	1	Cr[7:4]												Cr[3:0]																							
		2	Y[7:4]												Y[3:0]																							
Pins D[35:0]			35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

An input format of YCbCr 4:2:2 DDR can be selected by setting the input ID (0x15 [3:0]) to 0x6. The three different input pin assignment styles are shown in the table. The Input Style can be set in 0x16[3:2]. The data bit width (12, 10, or 8 bits) must be set with 0x16 [5:4]. The Data Input Edge is defined in 0x16 [1]. The 1st and the 2nd edge may be the rising or falling edge. The Data Input Edge is defined in 0x16 [1]. 0b1 = 1st edge rising edge; 0b0 = 1st edge falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

Figure 3 DDR DE timing - Register 0x16[1] = 1

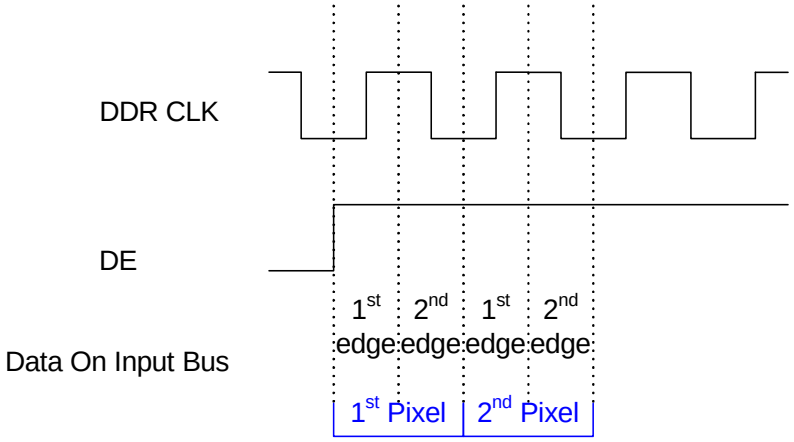
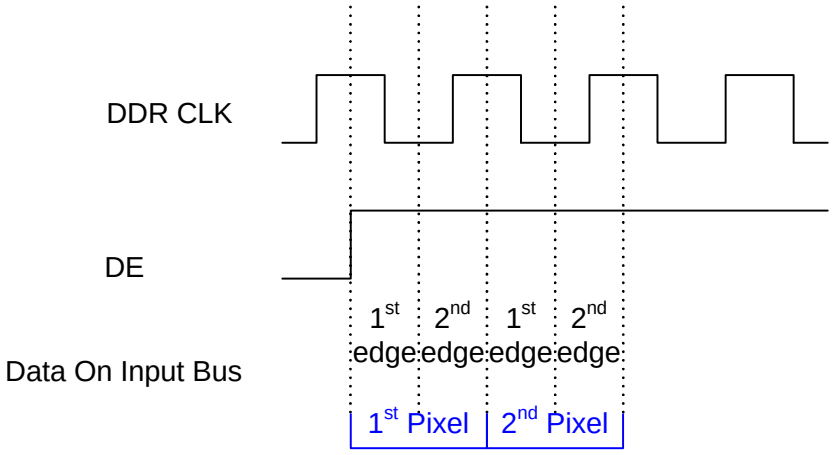


Figure 4 DDR DE timing - Register 0x16[1] = 0



4.3.2.1 Input Data Clock

When using an input format where the clock is 2 or 4 times the frequency of the data, such as 480i at 27MHz, CLK Divide register bits (0x9D[3:2]) and the CLK Divide Reset Register bit (0xA4[6]) need to be set accordingly. ► Figure 5 illustrates this function. The generated clock can be synchronized to the Hsync, Vsync, or DE. This can be selected in register bits 0xD0[3:2].

Register 0xBA controls the clock delay for the video data capture. For DDR, the negative edge clock delay can be controlled independently of the positive edge. To enable independent, negative-edge DDR control, set 0xD0[7] to 1. The delay can be controlled in register bits 0xD0[6:4].

Figure 5 **Input Clock Divide Control**

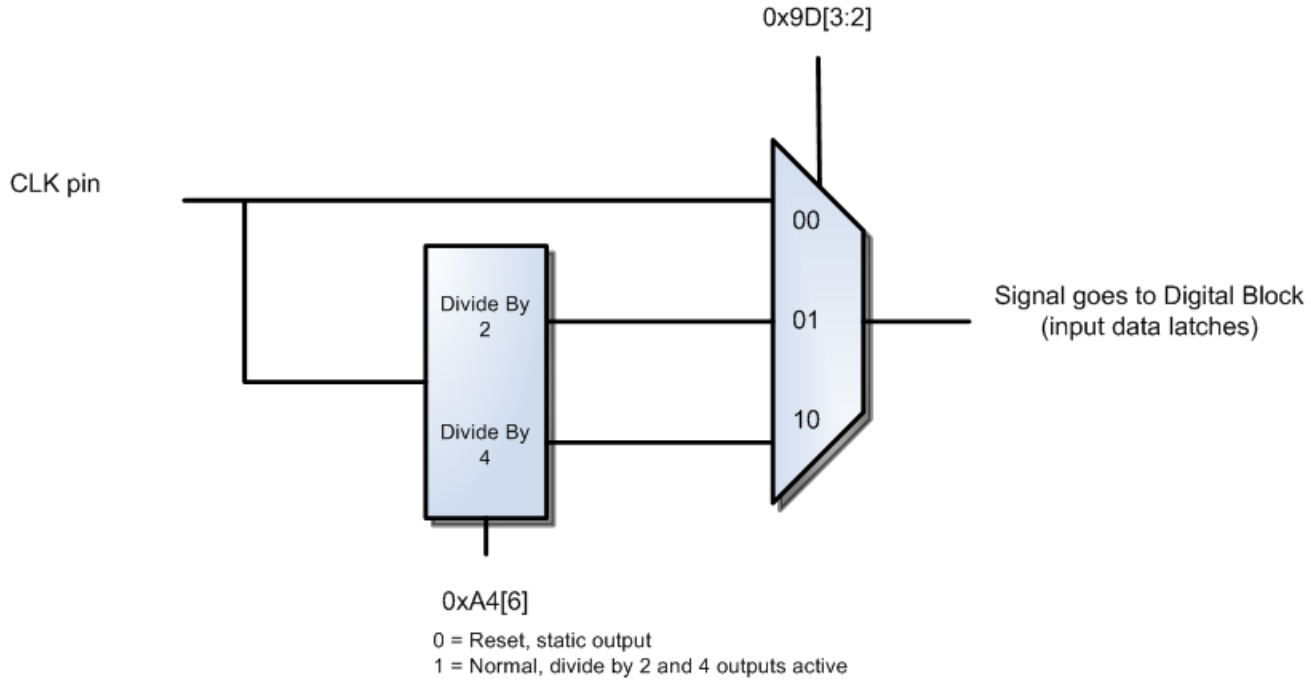


Table 28 Input Formatting Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x15	R/W	[3:0]	****0000	Input ID	Input Video Format See ►Table 16 to ►Table 27 0000 = 24 bit RGB 4:4:4 or YCbCr 4:4:4 (separate syncs) 0001 = 16, 20, 24 bit YCbCr 4:2:2 (separate syncs) 0010 = 16, 20, 24 bit YCbCr 4:2:2 (embedded syncs) 0011 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, separate syncs) 0100 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, embedded syncs) 0101 = 12, 15, 16 bit RGB 4:4:4 or YCbCr (DDR with separate syncs) 0110 = 8,10,12 bit YCbCr 4:2:2 (DDR with separate syncs) 0111 = 8, 10, 12 bit YCbCr 4:2:2 (DDR separate syncs) 1000 = 8, 10, 12 bit YCbCr 4:2:2 (DDR embedded syncs)
0x16	R/W	[7]	0*******	Output Format	Output Format 0 = 4:4:4 1 = 4:2:2
		[5:4]	**00****	Color Depth	Color Depth for Input Video Data. See ►Table 16 to ►Table 27 00 = invalid 10 = 12 bit 01 = 10 bit 11 = 8 bit
		[3:2]	****00**	Input Style	Styles refer to the input pin assignments. See ►Table 16 to ►Table 27 00 = Not Valid 01 = style 2 10 = style 1 11 = style 3
		[1]	******0*	DDR Input Edge	Video data input edge selection. Defines the first half of pixel data clocking edge. Used for DDR Input ID 5 and 6 only. 0 = falling edge 1 = rising edge
0x17	R/W	[6]	*0******	Vsync Polarity	Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through 1 = sync polarity invert 0 = High polarity 1 = Low polarity
		[5]	**0*****	Hsync Polarity	HSync polarity for Embedded Sync Decoder and Sync Adjustment Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through 1 = sync polarity invert 0 = High polarity 1 = Low polarity

Address	Type	Bits	Default Value	Register Name	Function
		[2]	*****0**	4:2:2 to 4:4:4 Interpolation Style	4:2:2 to 4:4:4 Up Conversion Method 0 = use zero order interpolation 1 = use first order interpolation
0x48	R/W	[6]	*0******	Video Input Bus Reverse	Bit order reverse for input signals. 0 = Normal Bus Order 1 = LSB .... MSB Reverse Bus Order
		[5]	**0*****	DDR Alignment	DDR alignment (Only For ID 5) See►Table 23 - ►Table 27 0 = DDR input is D[17:0] 1 = DDR input is D[35:18]
		[4:3]	***00***	Video Input Justification	Bit Justfication for YCbCr 4:2:2 modes. See►Table 17 to ►Table 22and ►Table 25 to ►Table 27 00 = evenly distributed 01 = right justified 10 = left justified 11 = Invalid
0xBA	R/W	[7:5]	000*****	Clock Delay	Programmable delay for input video clock. Default is 0 for no delay. 000 = -1.2ns 001 = -0.8ns 010 = -0.4ns 011 = no delay 100 = 0.4ns 101 = 0.8ns 110 = 1.2ns 111 = 1.6ns
0xD0	R/W	[7]	0*******	Enable DDR Negative Edge CLK Delay	Enable DDR Negative Edge Clock Delay Adjust 0 = Disable DDR Negative Edge CLK Delay 1 = Enable DDR Negative Edge CLK Delay
		[6:4]	*011****	DDR Negative Edge CLK Delay	Delay Adjust for the Input Video CLK Negative Edge for DDR Capture Should be set to 0b011 for No Delay 000 = -1200 ps 001 = -800 ps 010 = -400 ps 011 = no delay 100 = 400 ps 101 = 800 ps 110 = 1200 ps 111 = Invert CLK
		[3:2]	****00**	Sync Pulse Select	Case 1: Input ID register bits (0x15[3:0] = 5,6,7,8 Must be 0b11 Case 2: For input ID 1, 2, 3, 4 with 1X clock (See the Input Data Clock section, number 0). Can be set to any value. Case 3: For 2X or 4X input clock (See Input Data Clock section) with ID 1, 2, 3, 4. 1X generated clock synchronizes with. 00 = DE 01 = Hsync 10 = Vsync

Address	Type	Bits	Default Value	Register Name	Function
					11 = no sync pulse

4.3.3 Video Mode Detection

The video mode detection feature can inform the user of the CEA 861D defined Video Identification (VIC) of the video being input to the ADV7511, as well as some additional formats. If an 861D format is detected, the VIC code is contained in register 0x3E[7:2]. Some additional non-861D formats are contained in 0x3F[7:5]. Some information from the user is required to make the VIC determination for formats which can't be distinguished by the automatic detection system. The aspect ratio (0x17[1]) is used to distinguish between 861D video timing codes where aspect ratio is the only difference. The Low Refresh Rate bits (0xFB[2:1]) inform the detection logic that a low-frequency Vsync format is being used, and specify the refresh rate. These include 1080p with 24, 25, and 30Hz refresh rates. The High Refresh Rate bit (0xD5[3:2]) allows the detection circuit to identify modes with 2x or 4x the normal refresh rate. For 240p and 288p modes the number of total lines can be selected in 0x3F[4:3]. The VIC detected is also affected by pixel repeat; see ►4.3.4.

The detected VIC will be sent in the AVI InfoFrame unless pixel repetition is applied, causing the sent VIC to be different. To override the VIC detection, the pixel repeat mode must be set to manual by setting register 0x3B[6:5] to 0b10 or 0b11. The desired VIC is input into 0x3C[5:0]. The transmitter can support non-CEA 861D modes, but these will not be automatically detected. In this case the VIC should be 0.

Table 29 **Video Mode Detection Related Registers (Main Map)**

Address	Type	Bits	Default Value	Register Name	Function
0x17	R/W	[1]	******0*	Aspect Ratio	Aspect ratio of input video. 0 = 4:3 Aspect Ratio 1 = 16:9 Aspect Ratio
0x3D	RO	[5:0]	**000000	VIC to Rx	VIC sent to HDMI Rx and Used in the AVI InfoFrame Status (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9

Address	Type	Bits	Default Value	Register Name	Function
					101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use
0x3E	RO	[7:2]	000000**	VIC Detected	Input VIC Detected (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9

Address	Type	Bits	Default Value	Register Name	Function
					100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use
0x3F	RO	[7:5]	000*****	Auxiliary VIC Detected	This register is for video input formats that are not inside the 861D table. 000 = Set by Register 0x3E 001 = 240p Not Active 010 = 576i not active 011 = 288p not active 100 = 480i active 101 = 240p active 110 = 576i active 111 = 288p active
		[4:3]	***00***	Progressive Mode Information	Information about 240p and 288p modes. Case 1: 240p 01 = 262 lines 10 = 263 lines Case 2: 288p 01 = 312 lines 10 = 313 lines 11 = 314 lines
0x40	R/W	[7]	0*******	GC Packet Enable	GC Packet Enable 0 = GC Packet Disabled 1 = GC Packet Enabled
0x41	R/W	[1]	******0*	Sync Adjustment Enable	Enable Sync Adjustment 0 = Disabled 1 = Enabled
0xD5	R/W	[3:2]	****00**	High Refresh Rate Video	High Refresh Rate Video for VIC Detection

Address	Type	Bits	Default Value	Register Name	Function
					00 = normal refresh rate 01 = 2x refresh rate 10 = 4x refresh rate 11 = not valid
0xFB	R/W	[2:1]	*****00*	Low Refresh Rate (VIC Detection)	Low Refresh Rate indicates if input video VS refresh rate if it is less than 50Hz 00 = not low refresh rate 01 = 24Hz 10 = 25Hz 11 = 30Hz

4.3.4 Pixel Repetition

Pixel repetition is used in HDMI to increase the amount of blanking period available to send packets or to increase the pixel clock to meet the minimum specified clock frequency. The ADV7511 offers three choices for the user to implement this function: auto mode, manual mode, and max mode (0x3B[6:5]). If using SPDIF or I2S the ADV7511 can automatically select the necessary pixel repetition multiple for combinations of video format and audio sample rate. The video is converted to the appropriate format within the ADV7511, and the resulting VIC is sent in the AVI InfoFrame. Note that automatic pixel repeat does not work for HBR, DSD, and DST audio formats.

In automatic mode, the ADV7511 takes the audio sampling rate and detected VIC information as parameters to decide if pixel repeat is needed to obtain sufficient blanking periods to send the audio. For I2S, the sampling rate is determined by register 0x15. The audio sampling rate is either determined by the channel status information of the incoming SPDIF data, or by setting register 0x15. In the case of SPDIF, the source of the sampling rate information is set in register 0x0C[7]. With I2S, the sampling rate is always set by the user. If the pixel repetition factor is adjusted to meet bandwidth requirements, then the detected input VIC may be different from the VIC sent to the Rx. The VIC of the actual video sent, which is included in the AVI InfoFrame, can be seen in register 0x3D[5:0].

In the manual pixel repeat selection case, the VIC sent in the AVI info frame will need to be set in register 0x3C. The multiplication of the input clock must be programmed in 0x3B[6:5], and the pixel repeat value sent to the Rx must be programmed in 0x3B[4:3]. Refer to the ▹ *HDMI 1.3* specification for more details on valid pixel repeat formats.

Max mode works in the same way as the automatic mode, except that it will always select the highest pixel repeat multiple the HDMI Tx is capable of. This makes the video timing independent of the audio sampling rate. This mode is not typically used.

Table 30 Pixel Repetition Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x3B	R/W	[6:5]	*00*****	PR Mode	Pixel Repetition Mode Selection. Set to b00 unless non-standard video is supported. 00 = auto mode 01 = max mode 10 = manual mode 11 = manual mode
		[4:3]	***00***	PR PLL Manual	The clock multiplication of the input clock used in pixel repetition. 00 = x1 01 = x2 10 = x4 11 = x4
		[2:1]	*****00*	PR Value Manual	User programmed pixel repetition number to send to Rx. 00 = x1 01 = x2 10 = x4 11 = x4
0x3C	R/W	[5:0]	**000000	VIC Manual	User programmed VIC to sent to Rx (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9

Address	Type	Bits	Default Value	Register Name	Function
					011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use
0x3D	RO	[7:6]	00******	Pixel Repeat to Rx	The actual pixel repetition sent to Rx 00 = x1 01 = x2 10 = x4 11 = x4
		[5:0]	**000000	VIC to Rx	VIC sent to HDMI Rx and Used in the AVI InfoFrame Status (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3

Address	Type	Bits	Default Value	Register Name	Function
					001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use

4.3.5 422 444 Conversion

The ADV7511 can up-convert from 4:2:2 format to 4:4:4 format as well as down-convert from 4:4:4 to 4:2:2. To convert from 4:4:4 to 4:2:2, the video data always goes through a filter first to remove any artificial down-sampling noise. To convert from 4:2:2 to 4:4:4, the ADV7511 utilizes either the zero-order up-conversion (repetition) or first-order up-conversion (linear

interpolation). The type of interpolation, zero or first order, can be selected in register 0x17[2], and interpolation will give the best results.

The up-conversion and down-conversions are automatically applied when the video output format does not match the video input format. The input format is selected as described in ► 4.3.1, and the output format is selected in bits 0x16[7:6].

4.3.6 Deep Color Conversion

Deep Color Output can be selected by the GC CD register bit (0x4C[3:0]). The GC CD sets the output depth as well as the CD field in the general control packet. If the input video has less than the number of bits specified in GC CD, the extra LSBs will be filled with 0. When the input video has more information than the output, color depth bit trimming is automatically used. The method for color depth trimming can be selected using the Bit Trimming Mode register bits (0x49[7:2]). To enable Deep Color the General Control Packet must be enabled by setting the GC Packet Enable register bit 0x40[7] to 1.

To avoid a partial update of the General Control packet, the Packet Update features should be used. By setting the GC Packet Update register bit (0x48[4] Packet Memory) to 1, the current values for GC Header and Packet Bytes will be stored and sent in the GC Packets. The user should update the values then set the GC Packet Update register bit to '0' to begin sending the new packets. See section 4.2.5 for details.

Table 31 Deep Color Conversion Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x49	R/W	[7:2]	101010**	Bit Trimming Mode	Bit Trimming Mode All other settings are invalid 000000 = Active Dither 101010 = Truncate
0x4A	R/W	[4]	***0****	GC Packet Update	GC Packet Update: Before updating the GC Packet using I2C set to '1' to continue sending the current values. 0 = GC Packet I2C update inactive 1 = GC Packet I2C update active
0x4C	RO	[7:4]	0000****	GC PP	Pixel packing phase for Deep Color conversion. (Read Only)
		[3:0]	****0000	GC Packet - Color Depth	Color depth of video to Rx All other settings are invalid 0000 = Color Depth Not Indicated 0100 = 24 Bits/Pixel 0101 = 30 Bits/Pixel 0110 = 36 Bits/Pixel

4.3.7 DE, Hsync and Vsync Generation

When transmitting video data across the TMDS interface, it is necessary to have an Hsync, Vsync, and Data Enable (DE) defined for the image. There are three methods for sync input to the ADV7511. See ► Figure 6for a block diagram of the sync processing capabilities. For 3D formats extended MSBs for several DE, Hsync and Vsync generation fields have been added in registers 0xFA and 0xFB. For standard CEA861 formats, these registers can be left at default.

Separate Hsync, Vsync, and DE

For this method, all necessary signals are provided so neither Sync generation or DE generation is required. If desired, the

user can adjust the Hsync and Vsync timing relative to DE (refer to Hsync and Vsync adjustment section). Also, the DE timing can be adjusted relative to Hsync and Vsync. If both Hsync and Vsync adjustment and DE adjustment are chosen, the order can be selected. By setting register 0xD0[1] to 0, first the Hsync and Vsync is adjusted based on the input DE, then the DE timing is adjusted based on the new Hsync and Vsync. By setting register 0xD0[1] to 1, first the DE timing is adjusted based on the input Hsync and Vsync, then the Hsync and Vsync timing is adjusted based on the new DE.

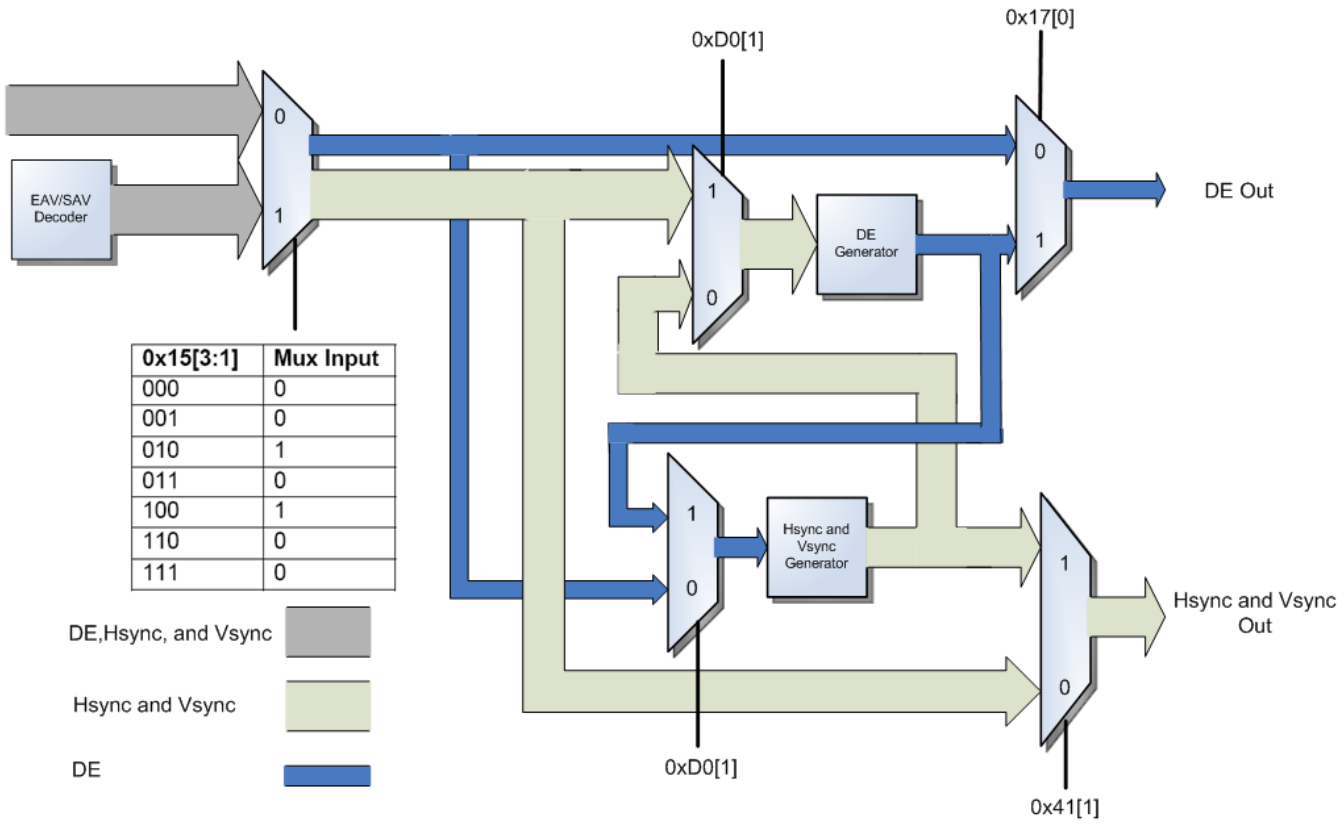
Embedded Syncs (SAV and EAV)

This method requires that Hsync and Vsync be generated. Registers 0x30 through 0x34 and 0x17[6:5] contain the settings for Hsync and Vsync generation in the embedded sync decoder section. The ADV7511 will use the signal generated by the EAV and SAV as the DE by default, but a new DE can also be generated. Sync adjustment is also available. If both Hsync and Vsync adjustment and DE adjustment are chosen, the orderin which they are implemented can be selected. By setting register 0xD0[1] to 0, first the Hsync and Vsync is adjusted based on the signal defined by the SAV and EAV, then the DE timing is generated based on the new Hsync and Vsync. This is useful if the interlace offset feature is desired, because it is available in the sync adjustment section, but not the embedded sync decoder section. By setting register 0xD0[1] to 1, first the DE timing is adjusted based on the Hsync and Vsync generated by the embedded sync decoder, then the Hsync and Vsync timing is adjusted based on the new DE.

Separate Hsync and Vsync only

This method requires that a DE be generated. Hsync and Vsync can also be adjusted based on the new DE if desired by enabling the Hsync and Vsync generation and setting the order to DE generation then Hsync Vsync Generation. This would be necessary if the location of the separate Hsync and Vsync were not in the same position relative to the data in the input signal, as the Hsync and Vsync defined in the CEA 861 are to the DE defined in the CEA 861.

Figure 6 Sync Processing Block Diagram



0x15[3:1]	Mux Input
000	0
001	0
010	1
011	0
100	1
110	0
111	0

4.3.7.1 DE generation

External Sync Input Modes

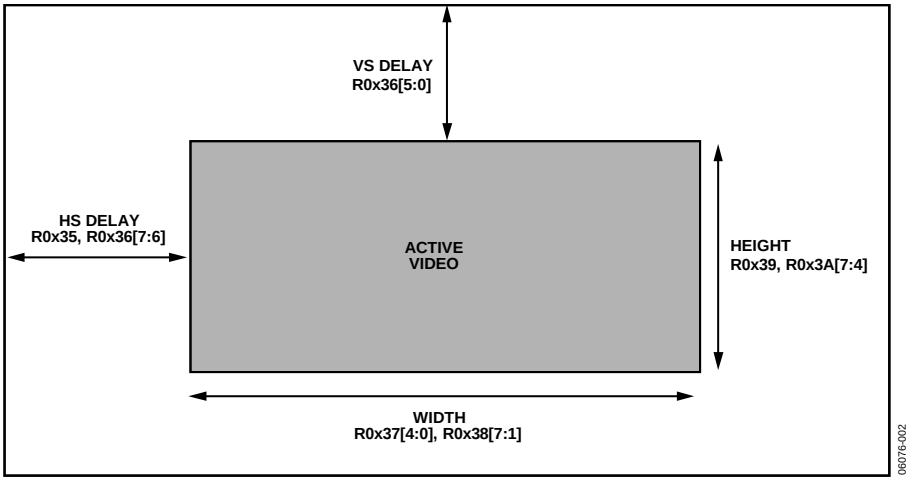
To properly frame the active video, the ADV7511 can use an external DE (via external pin) or can generate its own DE signal. To activate the internal DE generation, set register 0x17[0] to 1. Registers 0x35 – 0x3A and 0xFB are used to define the DE. Registers 0xFB[7],0x35 and 0x36[7:6] define the number of pixels from the Hsync leading edge to the DE leading edgeminus one. Registers 0xFB[6:5] and 0x36[5:0] is the number of Hsyncs between leading edge of VS and DE. Register 0x37[7:5] defines the difference of Hsync counts during Vsync blanking for the two fields in interlaced video. Registers 0xFB[4], 0x37[4:0] and 0x38[7:1] indicate the width of the DE. Registers 0x39 and 0x3A[7:4] are the number of lines of active video. These adjustments are illustrated in ► Figure 7.

Embedded Sync Input Mode

The F, H, and V codes from the embedded syncs define the DE by default in the ADV7511. To achieve 861D formats at the output by default, the embedded sync V signal needs to be aligned with the data as specified in the ▹ 861D specification.

The internal DE generator can also be enabled when using embedded syncs by setting register 0x17[0] to 1. The default reference point for the DE parameters are the Hsync and Vsync from the embedded sync decoder block which are defined by registers 0x30 – 0x34. The adjusted Hsync and Vsync output can also be used as the reference for DE generation if desired.

Figure 7 Active Video



4.3.7.2 Hsync and Vsync Generation

For video with embedded syncs, it is necessary to reconstruct the Hsync and Vsync. This is done with registers 0xFA, 0x30 – 0x34 and 0x17[6:5]. Registers 0xFA[7:5],0x30 and 0x31[7:6] specify the number of pixels between the Hsync leading edge and the trailing edge of DE. Registers 0x31[5:0] and 0x32[7:4] are the duration of the Hsync in pixel clocks. Registers 0x32[3:0] and 0x33[7:2] are the number of Hsync pulses between the trailing edge of the last DE and the leading edge of the Vsync pulse. Registers 0x33[1:0] and 0x34[7:0] are the duration of Vsync in units of Hsyncs. Hsync and Vsync polarity can be specified by setting registers 0x17[5] and 0x17[6]. ► Figure 8 –►Figure 10 show the sync generation parameters.

4.3.7.3 Hsync and Vsync Adjustment

Hsync and Vsync can also be adjusted based on a DE input, output of the embedded sync decoder, or output of the DE generator. Setting 0x41[1] to 1 enables this function. Registers 0xFA and 0xD8 – 0xDD set the Hsync and Vsync parameters. Register 0x17[6:5], shared with the embedded sync decoder, is used to set the polarity. For interlaced formats the Vsync placement is independent with each field. The Vsync Placement for interlaced fields is adjusted as shown in ► Figure 10, where Vsync Placement is set in registers 0xD9[3:0] and 0xDA[7:2], and offset is set in register 0xDC[7:5].

Figure 8 Hsync Reconstruction

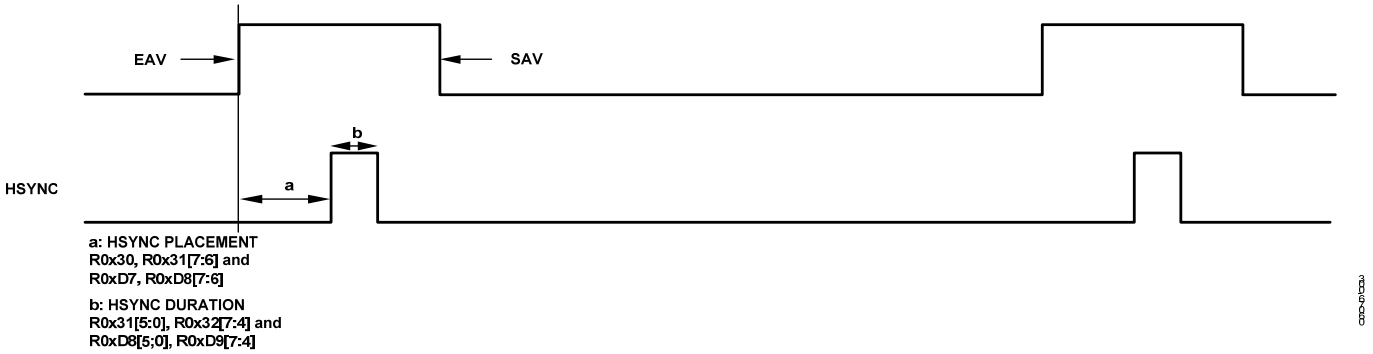


Figure 9 Vsync Reconstruction (centered)

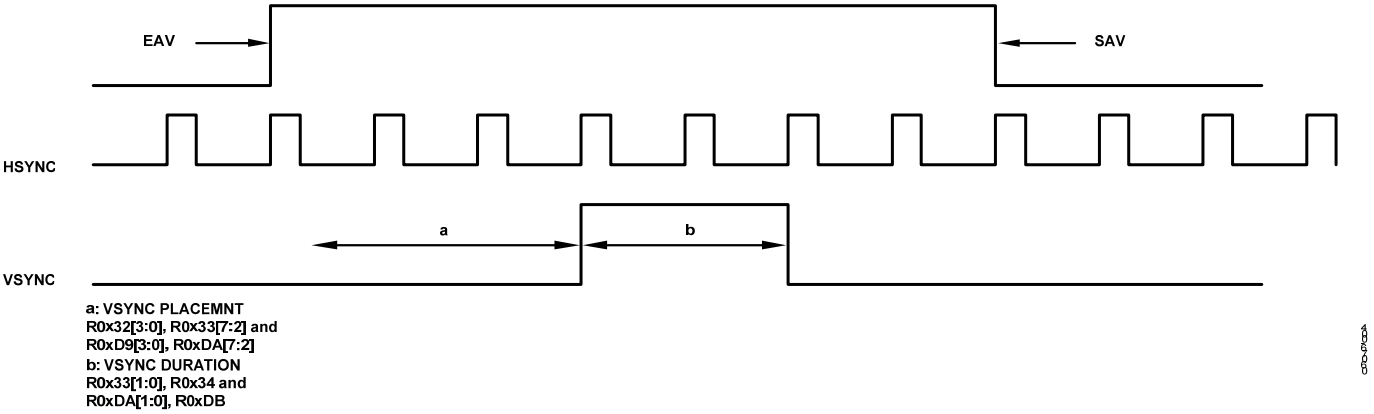
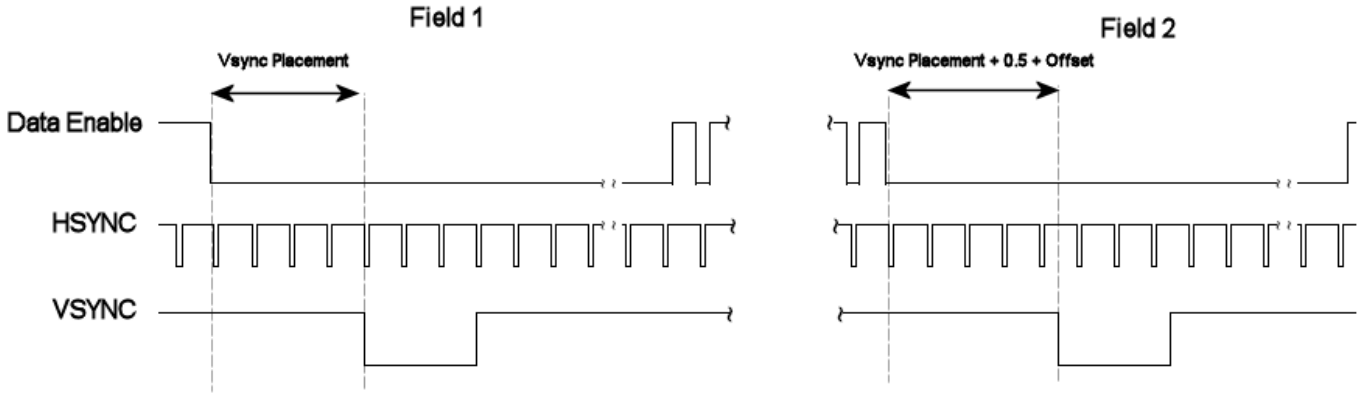


Figure 10 Sync Adjustment Vsync Offset (centered)



4.3.7.4 DE, Hsync, and Vsync Generation Recommended Settings

The following 4 tables show recommended settings for DE and Sync generation and adjustment. The settings are dependent on the video input, so these settings are intended to be used as a starting point. Some adjustments may be required from these settings to achieve a CEA861 compatible output.

Table 32 DE and HSync/Vsync Generation Common Format Settings

Format	Hsync Placement	Hsync Duration	Vsync Placement	Vsync Duration	Hsync Polarity	Vsync Polarity	Hsync Delay	Vsync Delay	Offset	Width	Height
480i	19	62	4	3	0	0	118	18	0	720	240
576i	12	63	2	3	0	0	131	22	0	720	288
480p	16	62	9	6	0	0	121	36	0	720	480
576p	12	64	5	5	0	0	131	44	0	720	576
720p-60	110	40	5	5	1	1	259	25	0	1280	720
720p-50	440	40	5	5	1	1	259	25	0	1280	720
1080i-30	88	44	2	5	1	1	191	20	0	1920	540
1080i-25	528	44	2	5	1	1	191	20	0	1920	540
1080p-60	88	44	4	5	1	1	191	41	0	1920	1080
1080p-50	528	44	4	5	1	1	191	41	0	1920	1080
1080p-24 (Frame Packing)	638	44	4	5	1	1	191	41	0	1920	2205
720p-60 (Frame Packing)	110	40	5	5	1	1	259	25	0	1280	1470
720p-50 (Frame Packing)	440	40	5	5	1	1	259	25	0	1280	1470

Table 33 Register Settings for DE Generation

Register (Main Map)	0x35	0x36	0x37	0x38	0x39	0x3A
720p - 50	0x40	0xD9	0x0A	0x00	0x2D	0x00
720p – 60	0x40	0xD9	0x0A	0x00	0x2D	0x00
480p	0x1E	0x64	0x05	0xA0	0x1E	0x00
480i	0x1D	0x92	0x05	0xA0	0x0F	0x00
1080i -25	0x2F	0xD4	0x0F	0x00	0x21	0xC0
1080i – 30	0x2F	0xD4	0x0F	0x00	0x21	0xC0
576p	0x20	0xEC	0x05	0xA0	0x24	0x00
576i	0x20	0xD6	0x05	0xA0	0x12	0x00
1080p-60	0x2F	0xE9	0x0F	0x00	0x43	0x80
1080p-50	0x2F	0xE9	0x0F	0x00	0x43	0x80
1080p-24 (Frame Packing)	0x2F	0xE9	0x0F	0x00	0x89	0xD0
720p-60 (Frame Packing)	0x40	0xD9	0x0A	0x00	0x5B	0xE0
720p-50 (Frame Packing)	0x40	0xD9	0x0A	0x00	0x5B	0xE0

Table 34 Register Settings for Sync Adjustment

Register (Main Map)	0xD7	0xD8	0xD9	0xDA	0xDB	0x17[6:5]
720p - 50	0x6E	0x02	0x80	0x14	0x05	0x0
720p – 60	0x1B	0x82	0x80	0x14	0x05	0x0
480p	0x04	0x03	0xE0	0x24	0x06	0x3
480i	0x04	0xC3	0xE0	0x10	0x03	0x3
1080i -25	0x84	0x02	0xC0	0x08	0x05	0x0
1080i – 30	0x16	0x02	0xC0	0x08	0x05	0x0
576p	0x03	0x04	0x00	0x14	0x05	0x3
576i	0x03	0x03	0xF0	0x08	0x03	0x3
1080p-60	0x16	0x02	0xC0	0x10	0x05	0x0
1080p-50	0x84	0x02	0xC0	0x10	0x05	0x0
1080p-24 (Frame Packing)	0x9F	0x82	0xC0	0x10	0x05	0x0
720p-60 (Frame Packing)	0x6E	0x02	0x80	0x14	0x05	0x0
720p-50 (Frame Packing)	0x1B	0x82	0x80	0x14	0x05	0x0

Table 35 Register Settings for Embedded Sync Processing

Register (Main Map)	0x30	0x31	0x32	0x33	0x34	0x17[6:5]
720p - 50	0x6E	0x02	0x80	0x14	0x05	0x0
720p – 60	0x1B	0x82	0x80	0x14	0x05	0x0
480p	0x04	0x03	0xE0	0x24	0x06	0x3
480i	0x04	0xC3	0xE0	0x10	0x03	0x3
1080i -25	0x84	0x02	0xC0	0x08	0x05	0x0
1080i – 30	0x16	0x02	0xC0	0x08	0x05	0x0
576p	0x03	0x04	0x00	0x14	0x05	0x3
576i	0x03	0x03	0xF0	0x08	0x03	0x3
1080p-60	0x16	0x02	0xC0	0x10	0x05	0x0
1080p-50	0x84	0x02	0xC0	0x10	0x05	0x0
1080p-24 (Frame Packing)	0x9F	0x82	0xC0	0x10	0x05	0x0
720p-60 (Frame Packing)	0x6E	0x02	0x80	0x14	0x05	0x0
720p-50 (Frame Packing)	0x1B	0x82	0x80	0x14	0x05	0x0

Table 36 DE, Hsync and Vsync Generation Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x17	R/W	[0]	*******0	DE Generator Enable	Enable DE Generator See registers 0x35 - 0x3A 0 = Disabled 1 = Enabled
0x30	R/W	[9:0]	00000000	Hsync Placement (Embedded Sync Decoder)	Upper 8 bits for Embedded Sync Decoder Hsync Placement (In Pixels)
0x31			00******		
0x31	R/W	[9:0]	**000000	Hsync Duration (Embedded Sync Decoder)	Upper 6 bit for Embedded Sync Decoder Hsync Duration (In Pixels)
0x32			0000****		
0x32	R/W	[9:0]	****0000	Vsync Placement (Embedded Sync Decoder)	Upper 4 bits for Embedded Sync Decoder Vsync Placement (In Hsyncs)
0x33			000000**		
0x33	R/W	[9:0]	******00	Vsync Duration (Embedded Sync Decoder)	Upper 2 bit for Embedded Sync Decoder Vsync Duration (In Hsyncs)
0x34			00000000		
0x35	R/W	[9:0]	00000000	Hsync Delay (DE Generator)	Upper 8 bits for DE Generation Hsync Delay (In Pixels)
0x36			00******		
0x36	R/W	[5:0]	**000000	Vsync Delay (DE Generator)	Vsync Delay for DE Generation. (In Hsyncs)
0x37	R/W	[7:5]	000*****	Interlace Offset (DE Generator)	Interlace Offset For DE Generation Sets the difference (in hsyncs) in field length between field 0 and field 1
0x37	R/W	[11:0]	***00000	Active Width (DE Generator)	Upper 5 bits for DE Generation Active Width (In Pixels)
0x38			0000000*		
0x39	R/W	[11:0]	00000000	Active Height (DE Generator)	Upper 8 bits for DE Generation Active Height (In Lines)

Address	Type	Bits	Default Value	Register Name	Function
0x3A			0000****		
0xD0	R/W	[1]	******0*	Timing Generation Sequence	Timing Generation Sequence 0 = sync adjustment then DE generation 1 = DE generation then sync adjustment
0xD7	R/W	[9:0]	00000000	Hsync Placement (Sync Adjustment)	Hsync Front Porch (In Pixels)
0xD8			00******		
0xD8	R/W	[9:0]	**000000	Hsync Duration (Sync Adjustment)	Hsync Duration (In Pixels)
0xD9			0000****		
0xD9	R/W	[9:0]	****0000	Vsync Placement (Sync Adjustment)	Vsync Front Porch (In Hsyncs)
0xDA			000000**		
0xDA	R/W	[9:0]	******00	Vsync Duration (Sync Adjustment)	Vsync Duration (In Hsyncs)
0xDB			00000000		
0xDC	R/W	[7:5]	000*****	Offset (Sync Adjustment)	Offset for Sync Adjustment Vsync Placement Used only with interlaced formats (In Hsyncs)
0xDC	R/W	[8:0]	***00000	Fixed	Must be default for proper operation;
0xDD			0000****		
0xFA	R/W	[7:5]	000*****	Hsync Placement MSB (Embedded Sync Decoding)	This is the MSB for Hsync Placment of Embedded Sync Decoding. See Register 0x35[7:0].
		[4:2]	***000**	Hsync Placement MSB (Sync Adjustment)	This is the MSB for Hsync Placment of Sync Adjustment. See Register 0xD7[7:0].
		[1:0]	******00	Fixed	Must be default for proper operation.
0xFB	R/W	[7]	0*******	Hsync Delay MSB (DE Generation)	MSB for Hsync delay of DE generation. See Register 0x35[7:0]
		[6:5]	*00*****	Vsync Delay MSB(DE Generation)	MSB for Vsync delay of DE generation. See Register bits 0x36[5:0]
		[4]	***0****	Width MSB (DE Generation)	MSB for DE width of DE generation. See Register bits 0x37[4:0]
		[3]	****0***	Height MSB (DE Generation)	MSB for height of DE generation. See Register bits 0x39[7:0]

4.3.8 Color Space Converter (CSC)

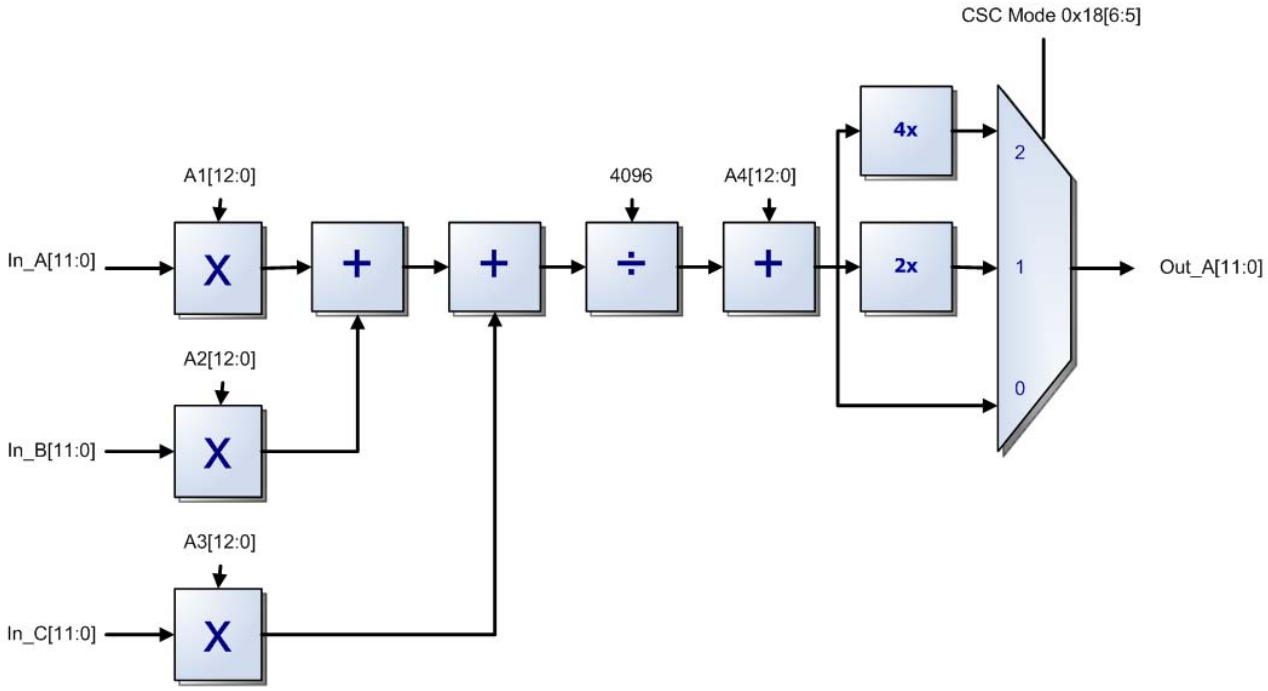
The color space converter (CSC) is a flexible 3x3 matrix that is capable of converting between a wide variety of color spaces. This section contains full details on the function of the CSC and register settings for common conversions.

4.3.8.1 Color Space Conversion (CSC) Matrix

The color space conversion (CSC) matrix in the ADV7511 is a 3 x 3 matrix with full programmability of all coefficients in the matrix. Each coefficient is 13 bit 2s complement to ensure that signal integrity is maintained. The CSC is designed to run at pixel rates of up to 170MHz. With the "any-to-any" color space conversion capability, formats such as RGB, YUV, YCbCr and others are supported by the CSC.

The CSC contains three identical processing channels, one of these is shown in ► Figure 11. The main inputs, In_A, In_B, and In_C, come from inputs to the ADV7511. Each input to the individual channels to the CSC is multiplied by a separate coefficient. In ► Figure 11these coefficients are marked A1, A2, and A3. The variable labeled A4 in ► Figure 11 is used as an offset control for Channel A in the CSC. The functional diagram for a single channel in the CSC, as per ► Figure 11, is repeated for the other two remaining channels, B and C. The coefficients for these channels are called B1, B2, B3, B4, C1, C2, C3 and C4.

Figure 11 Single CSC channel



The equations performed by the CSC are detailed as follows:

Equation 1: CSC Channel A

$$Out\_A = \left[In\_A\frac{A1}{4096} + In\_B\frac{A2}{4096} + In\_C\frac{A3}{4096} + A4 \right] 2^{CSC\_Mode}$$

Equation 2: CSC Channel B

$$Out\_B = \left[In\_A\frac{B1}{4096} + In\_B\frac{B2}{4096} + In\_C\frac{B3}{4096} + B4 \right] 2^{CSC\_Mode}$$

Equation 3: CSC Channel C

$$Out\_C = \left[In\_A\frac{C1}{4096} + In\_B\frac{C2}{4096} + In\_C\frac{C3}{4096} + C4 \right] 2^{CSC\_Mode}$$

As can be seen from *Equations 1-3*, the *A1-A3, B1-B3*, and *C1- C3* coefficients are used to scale the primary inputs. The values of A4, B4 and C4 are then added as offsets. The CSC Mode bits (register 0x18[6:5]) allow the user to implement conversion formulas in which the conversion coefficients are ≥ 1. In other words, if an equation is being implemented whose coefficients are ≥ 1, the CSC Mode bits can be used to ensure that the resulting output code does not exceed the 12-bit limit of 4095. ► Table 37 describes the conditions under which each CSC Mode setting should be used. Note that if any coefficient in any of the three CSC equations requires scaling (CSC Mode ≠ 0), then all coefficients, including the offset values, are scaled as indicated by *Equations 1 - 3*. The values of A1 - A4, B1 - B4, and C1 - C4 will equal the coefficients from the desired conversion formula multiplied by $\frac{4096}{2^{CSCMode}}$.

►Table 65 contains the register descriptions for all of the CSC control registers.

Table 37 CSC Mode Settings

CSC Mode	Conversion Coefficient
00	N < 1
01	1 ≤ N <2
10	2 ≤ N < 4

It should be noted that, in order for the CSC to operate properly, the channel mapping shown in ► Table 38 must be followed.

Table 38 CSC Port Mapping

Channel	CSC Channel
Red/Cr	A
Green/Y	B
Blue/Cb	C

Table 39 **HDTV YCbCr (Limited Range) to RGB (Limited Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xAC	0x53	0x08	0x00	0x00	0x00	0x19	0xD6
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1C	0x56	0x08	0x00	0x1E	0x88	0x02	0x91
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFF	0x08	0x00	0x0E	0x85	0x18	0xBE

Table 40 **HDTV YCbCr (Limited Range) to RGB (Full Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1C	0x1E	0x1F
Value	0xE7	0x34	0x04	0xAD	0x00	0x00	0x1C	0x1B
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1D	0xDC	0x04	0xAD	0x1F	0x24	0x01	0x35
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x04	0xAD	0x08	0x 7C	0x1B	0x77

Table 41 **SDTV YCbCr (Limited Range) to RGB (Limted Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xAA	0xF8	0x08	0x00	0x00	0x00	0x1A	0x84
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1A	0x6A	0x08	0x00	0x1D	0x50	0x04	0x23
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFC	0x08	0x00	0x0D	0xDE	0x19	0x13

Table 42 **SDTV YCbCr (Limited Range) to RGB (Full Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xE6	0x69	0x04	0xAC	0x00	0x00	0x1C	0x81
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1C	0xBC	0x04	0xAD	0x1E	0x6E	0x02	0x20
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFE	0x04	0xAD	0x08	0x1A	0x1B	0xA9

Table 43 **RGB (Limited Range) to HDTV YCbCr (Limited Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x88	0x2E	0x18	0x93	0x1F	0x3F	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x03	0x67	0x0B	0x71	0x01	0x28	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1E	0x21	0x19	0xB2	0x08	0x2D	0x08	0x00

Table 44 **RGB (Full Range) to HDTV YCbCr (Limited Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x86	0xFF	0x19	0xA6	0x1F	0x5B	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x02	0xE9	0x09	0xCB	0x00	0xFD	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1E	0x66	0x1A	0x9B	0x06	0xFF	0x08	0x00

Table 45 **RGB (Limted Range) to SDTV YCbCr (Limited Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x88	0x2E	0x19	0x26	0x1E	0xAC	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x04	0xC9	0x09	0x65	0x01	0xD2	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1D	0x3F	0x1A	0x93	0x08	0x2E	0x08	0x00

Table 46 **RGB (Full Range) to SDTV YCbCr (Limited Range)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x86	0xFF	0x1A	0x24	0x1E	0xDD	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x04	0x18	0x08	0x0A	0x01	0x8F	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1D	0xA5	0x1B	0x5C	0x06	0xFF	0x08	0x00

Table 47 **HDTV YCbCr (Limited Range) to SDTV YCbCr (Limited Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA7	0xDD	0x00	0x00	0x1F	0x6C	0x00	0x5B
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x01	0x88	0x08	0x00	0x00	0xCB	0x1E	0xD6
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0x1D	0x00	0x00	0x07	0xEB	0x00	0x7B

Table 48 **HDTV YCbCr (Limited Range) to SDTV YCbCr (Full Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA8	0xEB	0x00	0x00	0x1F	0x58	0x1F	0xDE
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x01	0xC9	0x09	0x50	0x00	0xEC	0x1F	0x25
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1E	0xFF	0x00	0x00	0x08	0xFA	0x03	0x1F

Table 49 **SDTV YCbCr (Limited Range) to HDTV YCbCr (Limited Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA8	0x33	0x00	0x00	0x00	0x99	0x1F	0x99
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1E	0x56	0x08	0x00	0x1F	0x13	0x01	0x4B
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0xEA	0x00	0x00	0x08	0x26	0x1F	0x78

Table 50 **SDTV YCbCr (Full Range) to HDTV YCbCr (Limited Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xC3	0x9D	0x00	0x00	0x00	0x43	0x0F	0x26
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1F	0x44	0x03	0x6F	0x1F	0x97	0x00	0xD2
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x67	0x00	0x00	0x03	0x97	0x00	0x4D

Table 51 **SDTV YCbCr (Limited Range) to SDTV YCbCr (Full Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA9	0x1B	0x00	0x00	0x00	0x00	0x1F	0x6E
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x00	0x00	0x09	0x50	0x00	0x00	0x1F	0x6B
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x00	0x00	0x09	0x1B	0x1F	0x6E

Table 52 **HDTV YCbCr (Full Range) to SDTV YCbCr (Limited Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x8E	0x0D	0x00	0x00	0x00	0x00	0x01	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x00	0x00	0x0D	0xBC	0x00	0x00	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x00	0x00	0x0E	0x0D	0x01	0x00

Table 53 **RGB (Full Range) to RGB (Limited Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x8D	0xBC	0x00	0x00	0x00	0x00	0x01	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x00	0x00	0x0D	0xBC	0x00	0x00	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x00	0x00	0x0D	0xBC	0x01	0x00

Table 54 **RGB (Limited Range) to RGB (Full Range)**

Register	A1		A2		A3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA9	0x50	0x00	0x00	0x00	0x00	0x1F	0x6B
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x00	0x00	0x09	0x50	0x00	0x00	0x1F	0x6B
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x00	0x00	0x09	0x50	0x1F	0x6B

Table 55 **Identity Matrix (Input = Output)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA8	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x00	0x00	0x08	0x00	0x00	0x00	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x00	0x00	0x08	0x00	0x00	0x00

Table 56 **HDTV YCbCr (16to 235) to RGB (16to 235)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xAC	0x53	0x08	0x00	0x00	0x00	0x19	0xD6
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1C	0x56	0x08	0x00	0x1E	0x88	0x02	0x91
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFF	0x08	0x00	0x0E	0x85	0x18	0xBE

Table 57 **HDTV YCbCr (16to 235) to RGB (0 to 255)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1C	0x1E	0x1F
Value	0xE7	0x34	0x04	0xAD	0x00	0x00	0x1C	0x1B
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1D	0xDC	0x04	0xAD	0x1F	0x24	0x01	0x35
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x04	0xAD	0x08	0x 7C	0x1B	0x77

Table 58 **SDTV YCbCr (16to 235) to RGB (16 to 235)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xAA	0xF8	0x08	0x00	0x00	0x00	0x1A	0x84
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1A	0x6A	0x08	0x00	0x1D	0x50	0x04	0x23
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFC	0x08	0x00	0x0D	0xDE	0x19	0x13

Table 59 **SDTV YCbCr (16to 235) to RGB (0 to 255) - (Default Value)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xE6	0x69	0x04	0xAC	0x00	0x00	0x1C	0x81

Register	A 1		A 2		A 3		A4	
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x1C	0xBC	0x04	0xAD	0x1E	0x6E	0x02	0x20
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1F	0xFE	0x04	0xAD	0x08	0x1A	0x1B	0xA9

Table 60 **RGB (16 to 235) to HDTV YCbCr (16to 235)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x88	0x2E	0x18	0x93	0x1F	0x3F	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x03	0x67	0x0B	0x71	0x01	0x28	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1E	0x21	0x19	0xB2	0x08	0x2D	0x08	0x00

Table 61 **RGB (0 to 255) to HDTV YCbCr (16to 235)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x86	0xFF	0x19	0xA6	0x1F	0x5B	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x02	0xE9	0x09	0xCB	0x00	0xFD	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1E	0x66	0x1A	0x9B	0x06	0xFF	0x08	0x00

Table 62 **RGB (16 to 235) to SDTV YCbCr (16to 235)**

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x88	0x2E	0x19	0x26	0x1E	0xAC	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x04	0xC9	0x09	0x65	0x01	0xD2	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1D	0x3F	0x1A	0x93	0x08	0x2E	0x08	0x00

Table 63 RGB (0 to 255) to SDTV YCbCr (16to 235)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0x86	0xFF	0x1A	0x24	0x1E	0xDD	0x08	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x04	0x18	0x08	0x0A	0x01	0x8F	0x01	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x1D	0xA5	0x1B	0x5C	0x06	0xFF	0x08	0x00

Table 64 Identity Matrix (Output = Input)

Register	A 1		A 2		A 3		A4	
Address	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
Value	0xA8	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Register	B1		B2		B3		B4	
Address	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
Value	0x00	0x00	0x08	0x00	0x00	0x00	0x00	0x00
Register	C1		C2		C3		C4	
Address	0x28	0x29	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
Value	0x00	0x00	0x00	0x00	0x08	0x00	0x00	0x00

4.3.8.2 Color Space Converter (CSC) Special Features

The Colorspace Converter also has three special features. For the case where YCbCr with a code range from -128 to 127 is input, setting bit 0xD5[1] to 1 will shift the code ranges to 0 - 255. If the user requires a black image to be sent across the HDMI link register 0xD5[0] should be set to 1, and register 0x16[0] should be set according to the output colorspace. The black image can be useful for protecting copyrighted content during HDCP authentication.

The minimum and maximum values for Y and CbCr can be set using the register in ► Table 65. For RGB, only the Y value will be used. YCbCr and RGB are distinguished by using the Input Color Space register bit (0x16[0]). This can be useful to ensure that video codes do not stray outside of the specified range when using limited range RGB or YCbCr.

4.3.8.3 Changing the Color Space with Active Display

The Color Space Converter Enable register bit 0x18[7] can cause the video to become momentarily unstable. To avoid this, time the end of the I2C write to coincide with the back porch of the Vsync. The Vsync interrupt can be used to synchronize the I2C write.

Table 65 Color Space Converter (CSC) Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x16	R/W	[0]	*******0	Output Color Space	Output Color Space Selection Used for Black Image and Range Clipping 0 = RGB 1 = YCbCr
0x18	R/W	[7]	0*******	CSC Enable	Color Space Converter Enable 0 = CSC Disabled 1 = CSC Enabled

Address	Type	Bits	Default Value	Register Name	Function
		[6:5]	*10*****	CSC Scaling Factor	Color Space Converter Mode Sets the fixed point position of the CSC coefficients. Including the a4, b4, c4, offsets. 00 = +/- 1.0, -4096 - 4095 01 = +/- 2.0, -8192 - 8190 10 = +/- 4.0, -16384 - 16380 11 = +/- 4.0, -16384 - 16380
0x18	R/W	[12:0]	***00110	A1 (CSC)	Color space Converter (CSC) coefficient for equations: **Equation 1: CSC Channel A** $Out\_A = \left[In\_A\frac{A1}{4096} + In\_B\frac{A2}{4096} + In\_C\frac{A3}{4096} + A4 \right] 2^{CSC\_Mode}$ **Equation 2: CSC Channel B** $Out\_B = \left[In\_A\frac{B1}{4096} + In\_B\frac{B2}{4096} + In\_C\frac{B3}{4096} + B4 \right] 2^{CSC\_Mode}$ **Equation 3: CSC Channel C** $Out\_C = \left[In\_A\frac{C1}{4096} + In\_B\frac{C2}{4096} + In\_C\frac{C3}{4096} + C4 \right] 2^{CSC\_Mode}$
0x19			01100010		
0x1A	R/W	[5]	**0*****	Coefficient Update	There are 2 methods to update the coefficients. Method 1: When Coefficient Update is always 0, the coefficient will be updated directly. Method 2: When Coefficient Update is used, there are 3 steps for updating a) Set Coefficient Update = 1 to buffer the CSC Coefficients b) Set the new CSC Coefficients c) Set Coefficient Updated = 0 to enable the new CSC Coefficients at the next Vsync rising edge 0 = Update Complete 1 = Allow CSC Update
0x1A	R/W	[12:0]	***00100	A2 (CSC)	See description for registers 0x18 and 0x19
0x1B			10101000		
0x1C	R/W	[12:0]	***00000	A3 (CSC)	See description for registers 0x18 and 0x19
0x1D			00000000		
0x1E	R/W	[12:0]	***11100	A4 (CSC)	See description for registers 0x18 and 0x19
0x1F			10000100		
0x20	R/W	[12:0]	***11100	B1 (CSC)	See description for registers 0x18 and 0x19
0x21			10111111		
0x22	R/W	[12:0]	***00100	B2 (CSC)	See description for registers 0x18 and 0x19
0x23			10101000		
0x24	R/W	[12:0]	***11110	B3 (CSC)	See description for registers 0x18 and 0x19

Address	Type	Bits	Default Value	Register Name	Function
0x25			01110000		
0x26	R/W	[12:0]	***00010	B4 (CSC)	See description for registers 0x18 and 0x19
0x27			00011110		
0x28	R/W	[12:0]	***00000	C1 (CSC)	See description for registers 0x18 and 0x19
0x29			00000000		
0x2A	R/W	[12:0]	***00100	C2 (CSC)	See description for registers 0x18 and 0x19
0x2B			10101000		
0x2C	R/W	[12:0]	***01000	C3 (CSC)	See description for registers 0x18 and 0x19
0x2D			00010010		
0x2E	R/W	[12:0]	***11011	C4 (CSC)	See description for registers 0x18 and 0x19
0x2F			10101100		
0xD5	R/W	[1]	******0*	YCbCr Code Shift	YCbCr Code Shift 0 = Code Shift Disabled 1 = Code Shift Enabled
		[0]	*******0	Black Image	Black Image 0 = Black Image Disabled 1 = Black Image Enabled

Table 66 Color Space Converter (CSC) Related Registers (CEC Map)

Address	Type	Bits	Default Value	Register Name	Function
0xC0	R/W	[11:0]	****0000	Y or RGB Minimum	Minimum value for Y or RGB for video data clipping.
0xC1			00000000		
0xC2	R/W	[11:0]	****1111	Y or RGB Maximum	Maximum value for Y or RGB for video data clipping.
0xC3			11111111		
0xC4	R/W	[11:0]	****0000	CbCr Minimum	Minimum value for Cb/Cr for video data clipping
0xC5			00000000		
0xC6	R/W	[11:0]	****1111	CbCr Maximum	Maximum value for Cb/Cr for video data clipping.
0xC7			11111111		

4.3.9 Video InfoFrame and Other Video Related Packets

Video related InfoFrames include the AVI InfoFrame, MPEG InfoFrame, GMP Packet.

To avoid a partial update of the packets the Packet Update features should be used. By setting the Packet Update register bit to 1 the current values will be stored and sent in the packets. The user should update the values then set the Packet Update register bit to 0 to begin sending the new packets. See section 4.2.5 for details.

4.3.9.1 AVI InfoFrame

The AVI InfoFrame is sent to the receiver to help it determine the intended aspect ratio and other formatting parameters of the video being transmitted across the HDMI link. The Y1Y0 bits (0x55[6:5]), which tell the sink whether YCbCr 4:2:2,4:4:4 or RGB are sent, and the Picture Aspect Ratio bits (0x56[5:4]) are required fields. Other field data can be entered if the information is available.

The Active Format Information Status bit (0x55[4]) tells whether the Bar Information, Scan Information, Colorimetry, Non-uniform Picture Scaling, and Active Aspect Ratio fields contain valid information.

The Active Format Aspect Ratio bits (0x56[3:0]) give the receiver useful information about the video that can be used to improve the picture. The Active Format Description code from the ETSI TR 101 151 version 1.4.1 Digital Video Broadcasting Specification, which is mentioned in ▹ *CEA 861D*, should be entered into this field. Additional formats can be entered manually in the bar information fields.

Registers 0x5A – 0x61 tell the receiver if there are black bars included in the video stream. Register 0x55[3:2] tells the receiver which bar information is valid: none, horizontal, vertical, or both.

To make sure theAVI InfoFrame information isn't partially sent while being updated the packet update feature can be used. The AVI Packet Update register bit (0x48[6]), should be set to 1, then the AVI Packet Registers written, and finally set back to 0. See section 4.2.5 for details.

Table 67 AVI InfoFrame Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x44	R/W	[4]	***1****	AVI InfoFrame Enable	AVI InfoFrame Enable 0 = Disabled 1 = Enabled
0x4A	R/W	[7]	1*******	Auto Checksum Enable	Auto Checksum Enable 0 = Use checksum from registers 1 = Use automatically generated checksum
		[6]	*0******	AVI Packet Update	AVI Packet Update: Before updating the AVI Packet using I2C set to '1' to continue sending the current values. 0 = AVI Packet I2C update inactive 1 = AVI Packet I2C update active
0x52	R/W	[2:0]	*****010	AVI InfoFrame Version	Version of AVI InfoFrame Should be left default
0x53	R/W	[4:0]	***01101	AVI InfoFrame Length	Length of packet body, excluding checksum
0x54	R/W	[7:0]	00000000	AVI InfoFrame Checksum	Checksum for AVI IF. Only used in manual checksum mode..
0x55	R/W	[7]	0*******	AVI Byte 1 bit 7	Reserved per HDMI spec. - set to 0
		[6:5]	*00*****	Y1Y0 (AVI InfoFrame)	Output format - this should be written when 0x16[7:6] is written. 00 = RGB 01 = YCbCr 4:2:2 10 = YCbCr 4:4:4 11 = reserved
		[4]	***0****	Active Format Information Status (AVI InfoFrame)	Active Format Information Present 0 = no data 1 = Active format Information valid
		[3:2]	****00**	Bar Information (AVI InfoFrame)	B[1:0] 00 = invalid bar 01 = vertical 10 = horizontal 11 = Both
		[1:0]	******00	Scan Information (AVI InfoFrame)	S[1:0] 00 = no data 01 = TV 10 = PC 11 = None
0x56	R/W	[7:6]	00******	Colorimetry (AVI InfoFrame)	C[1:0] 00 = no data 01 = ITU601 10 = ITU709 11 = Extended Colorimetry Information Valid (Indicated in register 0x57[6:4])
		[5:4]	**00****	Picture Aspect Ratio (AVI InfoFrame)	M[1:0] 00 = no data 01 = 4:3

Address	Type	Bits	Default Value	Register Name	Function
					10 = 16:9 11 = None
		[3:0]	****0000	Active Format Aspect Ratio (AVI InfoFrame)	R[3:0] 1000 = Same as Aspect Ratio 1001 = 4:3 (center) 1010 = 16:9 (center) 1011 = 14:9 (center)
0x57	R/W	[7]	0*******	ITC	IT Content 0 = None 1 = IT content available in register bits 0x59[5:4]
		[6:4]	*000****	EC[2:0]	E[2:0] All other values reserved per HDMI 1.4 Specification 000 = xvYCC 601 001 =xvYCC 709 010 = sYCC601 011 = AdobeYCC601 100 = AdobeRGB
		[3:2]	****00**	Q[1:0]	RGB Quantization range 00 = default range 01 = limited range 10 = full range 11 = reserved
		[1:0]	******00	Non-Uniform Picture Scaling (AVI InfoFrame)	SC[1:0] 00 = unknown 01 = scaling in Horizontal direction 10 = scaling in Vertical direction 11 = scaling in Both H & V directions
0x58	R/W	[7]	0*******	Byte 4 Bit 7 (AVI InfoFrame)	Reserved per HDMI spec. Set to '0'.
0x59	R/W	[7:4]	0000****	Byte 5 bit [7:4] (AVI InfoFrame)	YQ[1:0] 00 = Limited Range 01 = Full Range 10 = Reserved 11 = Reserved
0x5A	R/W	[7:0]	00000000	Active Line Start LSB (AVI InfoFrame)	Active Line Start This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.
0x5B	R/W	[7:0]	00000000	Active Line Start MSB (AVI InfoFrame)	Active Line Start This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.
0x5C	R/W	[7:0]	00000000	Active Line End LSB (AVI InfoFrame)	Active Line End This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.

Address	Type	Bits	Default Value	Register Name	Function
0x5D	R/W	[7:0]	00000000	Active Line End MSB (AVI InfoFrame)	Active Line End This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.
0x5E	R/W	[7:0]	00000000	Active Pixel Start LSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.
0x5F	R/W	[7:0]	00000000	Active Pixel Start MSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.
0x60	R/W	[7:0]	00000000	Active Pixel End LSB (AVI InfoFrame)	Active Pixel End This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.
0x61	R/W	[7:0]	00000000	Active Pixel End MSB (AVI InfoFrame)	Active Pixel End This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.
0x62	R/W	[7:0]	00000000	Byte 14 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x63	R/W	[7:0]	00000000	Byte 15 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x64	R/W	[7:0]	00000000	Byte 16 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x65	R/W	[7:0]	00000000	Byte 17 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x66	R/W	[7:0]	00000000	Byte 18 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x67	R/W	[7:0]	00000000	Byte 19 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x68	R/W	[7:0]	00000000	Byte 20 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x69	R/W	[7:0]	00000000	Byte 21 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6A	R/W	[7:0]	00000000	Byte 22 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6B	R/W	[7:0]	00000000	Byte 23 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6C	R/W	[7:0]	00000000	Byte 24 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6D	R/W	[7:0]	00000000	Byte 25 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6E	R/W	[7:0]	00000000	Byte 26 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.
0x6F	R/W	[7:0]	00000000	Byte 27 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.

4.3.9.2 MPEG InfoFrame

The MPEG InfoFrame is defined in ▹ *CEA 861D*. Currently, the specification does not recommend using this InfoFrame. Register 0x40[5] tells the ADV7511 whether or not to send the MPEG InfoFrame.

The contents of the MPEG InfoFrame are set in the Packet Memory. The device address for the Packet Memory map is programmable and is controlled by register 0x45 of the primary register map. The default setting is 0x70.

To make sure theMPEG InfoFrame information isn't partially sent while being updated the packet update feature can be used. See section 4.2.5 for details.

Table 68 MPEG InfoFrame Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[5]	**0*****	MPEG Packet Enabled	MPEG Packet Enable 0 = Disabled 1 = enable
0x4A	R/W	[7]	1*******	Auto Checksum Enable	Auto Checksum Enable 0 = Use checksum from registers 1 = Use automatically generated checksum

Table 69 MPEG InfoFrame Related Registers (Packetmemory Map)

Address	Type	Bits	Default Value	Register Name	Function
0x20	R/W	[7:0]	00000000	MPEG Header Byte 0	
0x21	R/W	[7:0]	00000000	MPEG Header Byte 1	
0x22	R/W	[7:0]	00000000	MPEG Header Byte 2	
0x23	R/W	[7:0]	00000000	MPEG Packet Byte 0	
0x24	R/W	[7:0]	00000000	MPEG Packet Byte 1	
0x25	R/W	[7:0]	00000000	MPEG Packet Byte 2	
0x26	R/W	[7:0]	00000000	MPEG Packet Byte 3	
0x27	R/W	[7:0]	00000000	MPEG Packet Byte 4	
0x28	R/W	[7:0]	00000000	MPEG Packet Byte 5	
0x29	R/W	[7:0]	00000000	MPEG Packet Byte 6	
0x2A	R/W	[7:0]	00000000	MPEG Packet Byte 7	
0x2B	R/W	[7:0]	00000000	MPEG Packet Byte 8	
0x2C	R/W	[7:0]	00000000	MPEG Packet Byte 9	
0x2D	R/W	[7:0]	00000000	MPEG Packet Byte 10	
0x2E	R/W	[7:0]	00000000	MPEG Packet Byte 11	
0x2F	R/W	[7:0]	00000000	MPEG Packet Byte 12	
0x30	R/W	[7:0]	00000000	MPEG Packet Byte 13	
0x31	R/W	[7:0]	00000000	MPEG Packet Byte 14	
0x32	R/W	[7:0]	00000000	MPEG Packet Byte 15	
0x33	R/W	[7:0]	00000000	MPEG Packet Byte 16	
0x34	R/W	[7:0]	00000000	MPEG Packet Byte 17	
0x35	R/W	[7:0]	00000000	MPEG Packet Byte 18	

Address	Type	Bits	Default Value	Register Name	Function
0x36	R/W	[7:0]	00000000	MPEG Packet Byte 19	
0x37	R/W	[7:0]	00000000	MPEG Packet Byte 20	
0x38	R/W	[7:0]	00000000	MPEG Packet Byte 21	
0x39	R/W	[7:0]	00000000	MPEG Packet Byte 22	
0x3A	R/W	[7:0]	00000000	MPEG Packet Byte 23	
0x3B	R/W	[7:0]	00000000	MPEG Packet Byte 24	
0x3C	R/W	[7:0]	00000000	MPEG Packet Byte 25	
0x3D	R/W	[7:0]	00000000	MPEG Packet Byte 26	
0x3E	R/W	[7:0]	00000000	MPEG Packet Byte 27	
0x3F	R/W	[7]	0*******	MPEG Packet Update	MPEG Packet Update: Before updating the MPEG Packet using I2C set to '1' to continue sending the current values. 0 = MPEG Packet I2C update inactive 1 = MPEG Packet I2C update active

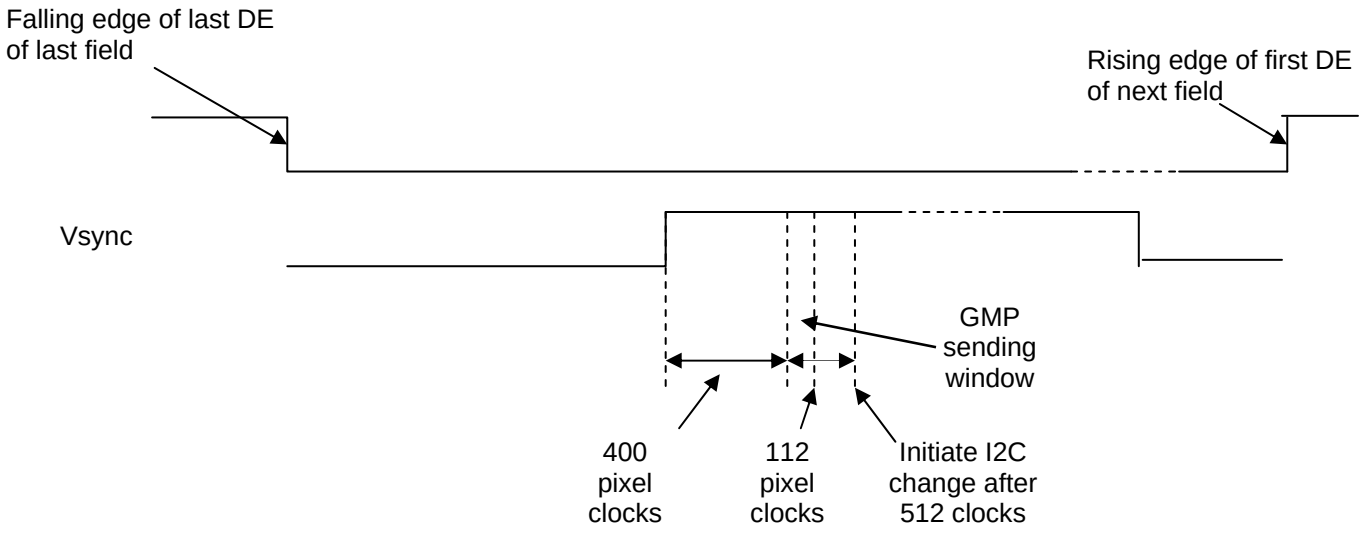
4.3.9.3 Gamut Metadata Packet

The Gamut Metadata Packet (GMP) contains the sources Gamut Boundary Description. It is defined in the ▹ *HDMI 1.3a* specification.

The contents of the GMP InfoFrame are set in the Packet Memory. The device address for the Packet Memory map is programmable and is controlled by register 0x45 of the primary register map. The default setting is 0x70. Transmission of the GMP data over the HDMI link is enabled by setting the GMP Enable bit (0x40[2] of the Main Register Map) to 1.

The ADV7511 transmits the GMP data starting 400 pixel clock cycles after the leading edge of Vsync. In order to update the GMP at the expected frame, it is recommended that the user set the packet update bit to 0 after the 512th pixel clock cycle after the Vsync leading edge. The Vsync interrupt of the ADV7511 should be used to synchronize this timing. ► Figure 12illustrates this GM Packet timing.

Figure 12 I2C Write Timing of GMP Data



The Packet Update feature can be used to ensure that the GMP Infoframe information is not partially sent while being updated. The GM Packet Update register bit (0xBF[7]), should be set to 1, then the GM Packet Registers written, and finally set back to 0. See section 4.2.5 for details.

Table 70 Gamut Metadata Packet Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[2]	*****0**	GM Packet Enable	GM Packet Enable 0 = Disabled 1 = Enabled

Table 71 Gamut Metadata Packet Related Registers (Packetmemory Map)

Address	Type	Bits	Default Value	Register Name	Function
0xA0	R/W	[7:0]	00000000	GM Header Byte 0	
0xA1	R/W	[7:0]	00000000	GM Header Byte 1	
0xA2	R/W	[7:0]	00000000	GM Header Byte 2	
0xA3	R/W	[7:0]	00000000	GM Packet Byte 0	
0xA4	R/W	[7:0]	00000000	GM Packet Byte 1	
0xA5	R/W	[7:0]	00000000	GM Packet Byte 2	
0xA6	R/W	[7:0]	00000000	GM Packet Byte 3	
0xA7	R/W	[7:0]	00000000	GM Packet Byte 4	
0xA8	R/W	[7:0]	00000000	GM Packet Byte 5	
0xA9	R/W	[7:0]	00000000	GM Packet Byte 6	
0xAA	R/W	[7:0]	00000000	GM Packet Byte 7	
0xAB	R/W	[7:0]	00000000	GM Packet Byte 8	
0xAC	R/W	[7:0]	00000000	GM Packet Byte 9	
0xAD	R/W	[7:0]	00000000	GM Packet Byte 10	
0xAE	R/W	[7:0]	00000000	GM Packet Byte 11	
0xAF	R/W	[7:0]	00000000	GM Packet Byte 12	
0xB0	R/W	[7:0]	00000000	GM Packet Byte 13	
0xB1	R/W	[7:0]	00000000	GM Packet Byte 14	
0xB2	R/W	[7:0]	00000000	GM Packet Byte 15	
0xB3	R/W	[7:0]	00000000	GM Packet Byte 16	
0xB4	R/W	[7:0]	00000000	GM Packet Byte 17	
0xB5	R/W	[7:0]	00000000	GM Packet Byte 18	
0xB6	R/W	[7:0]	00000000	GM Packet Byte 19	
0xB7	R/W	[7:0]	00000000	GM Packet Byte 20	

Address	Type	Bits	Default Value	Register Name	Function
0xB8	R/W	[7:0]	00000000	GM Packet Byte 21	
0xB9	R/W	[7:0]	00000000	GM Packet Byte 22	
0xBA	R/W	[7:0]	00000000	GM Packet Byte 23	
0xBB	R/W	[7:0]	00000000	GM Packet Byte 24	
0xBC	R/W	[7:0]	00000000	GM Packet Byte 25	
0xBD	R/W	[7:0]	00000000	GM Packet Byte 26	
0xBE	R/W	[7:0]	00000000	GM Packet Byte 27	
0xBF	R/W	[7]	0*******	GM Packet Update	GM Packet Update: Before updating the GM Packet using I2C set to '1' to continue sending the current values. 0 = GM Packet I2C update inactive 1 = GM Packet I2C update active

4.3.10 3D Video Setup

When sending 3D video formats from the ADV7511, both the VIC in the AVI InfoFrame and the Vendor Specific InfoFrame must be setup.

4.3.10.1 VIC

The ADV7511 does not detect the VIC for 3D formats. The VIC must be programmed using the manual pixel repeat mode by setting 0x3B[6:5] to '10'. The VIC should be programmed in register bits 0x3C[5:0]. A list of VICs can be found in the CEA861 document.

4.3.10.2 Pixel Repeat

The Pixel repeat value should be set in register 0x3B[2:1] and 0x3B[4:3]. This will be 0 for most formats However, depending on the audio and video formats used, sometimes pixel repeat must be used to increase the bandwidth available for audio. Look at table 7-5 in HDMISpecification1.4 to determine the appropriate pixel repeat value for the 2D VIC and audio format, then look at ► Table 72 to select the an appropriate PR for the corresponding 3D structure.

Table 72 **Pixel Repeat Values for 3D Formats**

2D PR Value in table 7-5	Frame Packing PR Value	Side-by-Side (Half) PR Value	Top-and-Bottom PR Value	Field Alternative PR Value	Line Alternative PR Value	Side-by-Side (Full) PR Value	L + Depth PR Value	L + depth + Graphics + Graphics-depth PR Value
None	None	None	None	None	None	None	None	None
2X	None	2X	2X	None	None	None	None	None
4X	2X	4X	4X	2X	2X	2X	2X	None

4.3.10.3 Vendor Specific InfoFrame

Either Spare Packet 1 or Spare Packet 2 can be used to set up the Vendor Specific InfoFrame. For information about setting up the InfoFrame packet see section 8.2.3 of the HDMI 1.4a Specification. For details about how to program the spare packet see section ▸4.2.7of this Programming Guide.

4.4 Audio Setup

4.4.1 Input Format

ADV7511 is capable of receiving audio data in either I2S, SPDIF, DSD, DST, or HBR format for packetization and transmission over the HDMI interface.

Table 73 Audio Input Format Summary

Input				Output			
Audio Select 0x0A[6:4]	**Audio Mode 0x0A[3:2]**	**I2S Format 0x0C[1:0]**	**Data Pins**	**Clock Pins**	**Encoding**	**Format**	**Packet Type**
000	**	00	I2S[3:0]	Required:SCLK Optional:MCLK	Normal[1]	Standard I2S	Audio Sample Packet
000	**	01	I2S[3:0]	Required:SCLK Optional: MCLK	Normal	Right Justified	Audio Sample Packet
000	**	10	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	Left Justified	Audio Sample Packet
000	**	11	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	AES3 Direct	Audio Sample Packet
001	00	**	SPDIF	Optional: MCLK	Biphase Mark	IEC60958 or IEC61937	Audio Sample Packet
010	0*	**	DSD[5:0] & I2S[3:2] for DSD[7:6]	Required: DSD_CLK	Normal	DSD	One Bit Audio Sample Packet
010	1*	**	DSD[5:0] & I2S[3:2] for DSD[7:6]	Required: DSD_CLK	SDIF-3	DSD	One Bit Audio Sample Packet
011	00	**	I2S[3:0]	Required: MCLK	Biphase Mark	IEC61937	HBR Audio Stream Packet
011	01	00	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	Standard I2S	HBR Audio Stream Packet
011	01	01	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	Right Justified	HBR Audio Stream Packet
011	01	10	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	Left Justified	HBR Audio Stream Packet
011	01	11	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	AES3 Direct	HBR Audio Stream Packet
011	10	**	SPDIF	Required: MCLK	Biphase Mark	IEC61937	HBR Audio Stream Packet
011	11	00	SPDIF	Required: SCLK Optional: MCLK	Normal	Standard I2S	HBR Audio Stream Packet
011	11	01	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	Right Justified	HBR Audio Stream Packet
011	11	10	I2S[3:0]	Required: SCLK Optional: MCLK	Normal	Left Justified	HBR Audio Stream Packet
011	11	11	I2S[3:0]	Required: MCLK	Normal	IEC61937	HBR Audio Stream Packet
100	*0	**	DSD[5] = DST_FF DSD[4] = DST_D	Required: DSD_CLK	Normal	DST Normal	DST Audio Packet
100	01	**	DSD[5] = DST_FF DSD[4] = DST_D	Required: DSD_CLK	Normal	DST 2X	DST Audio Packet
100	11	**	DSD[5] = DST_FF DSD[4] = DST_D	Required: DSD_CLK	Normal	DST 1X (DDR)	DST Audio Packet

[1] Normal Encoding means data is captured on the rising edge of the data clock

Table 74 **Input Format Related Registers (Main Map)**

Address	Type	Bits	Default Value	Register Name	Function
0x04	RO	[7:4]	0000****	SPDIF Sampling Frequency	SPDIF Sampling Frequency from SPDIF Channel Status. 0000 = 44.1 kHz 0001 = N/A 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = N/A 0101 = N/A 0110 = N/A 0111 = N/A 1000 = 88.2 kHz 1001 = N/A 1010 = 96.0 kHz 1011 = N/A 1100 = 176.4 kHz 1101 = N/A 1110 = 192.0 kHz 1111 = N/A
0x0A	R/W	[6:4]	*000****	Audio Select	Audio Select All others invalid 000 = I2S 001 = SPDIF 010 = One Bit Audio (DSD) 011 = High Bit Rate (HBR Audio) 100 = DST 101 = N/A 110 = N/A 111 = N/A
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select Case 1: DSD (Audio Select register bits (0x0A[6:4] = 0b010)) 0X = DSD raw mode 1X = SDIF-3 mode Case 2: HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding Case 3: DST (Audio Select register bits (0x0A[6:4] = 0b100)) X0 = normal mode 01 = 2x clock 11 = 1x clock or DDR case 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding
		[1:0]	******01	MCLK Ratio	MCLK Ratio The ratio between the audio sampling frequency and the clock described using N and CTS 00 = 128xfs 01 = 256xfs

Address	Type	Bits	Default Value	Register Name	Function
					10 = 384xfs 11 = 512xfs
0x0B	R/W	[7]	0*******	SPDIF Enable	Enable or Disable SPDIF receiver 0 = disable 1 = Enabled
		[6]	*0******	Audio Clock Polarity	SPDIF MCLK, I2S SCLK, and DSD Clock Polarity Indicates edge where input data is latched 0 = rising edge 1 = falling edge
		[5]	**0*****	MCLK Enable	MCLK Enable 0 = MCLK internally generated 1 = MCLK is available
0x0C	R/W	[7]	1*******	Audio Sampling Frequency Select	Select source of audio sampling frequency for pixel repeat and I2S mode 4 0 = use sampling frequency from I2S stream 1 = use sampling frequency from I2C register
		[6]	*0******	Channel Status Override	Source of channel status bits when using I2S mode 4 0 = use channel status bits from I2S stream 1 = use channel status bits from I2C registers
		[5]	**1*****	I2S3 Enable	I2S3 enable for theI2S 3 pin. 0 = Disabled 1 = Enabled
		[4]	***1****	I2S2 Enable	I2S2 enable for the I2S 2 pin. 0 = Disabled 1 = Enabled
		[3]	****1***	I2S1 Enable	I2S1 enable for the 4 I2S 1 pin. 0 = Disabled 1 = Enabled
		[2]	*****1**	I2S0 Enable	I2S0 enable for the I2S 0 pin. 0 = Disabled 1 = Enabled
		[1:0]	******00	I2S Format	I2S Format 00 = Standard I2S mode 01 = right justified mode 10 = left justified mode 11 = AES3 direct mode
0x0D	R/W	[4:0]	***11000	I2S Bit Width	I2S Bit Width For right justified audio only. Default is 24. Not valid for widths greater than 24.
0x42	RO	[3]	****0***	I2S 32 Bit Mode Detect	I2S Mode Detections Shows the number of SCLK periods per LRCLK period. 0 = 32 bit mode detected

Address	Type	Bits	Default Value	Register Name	Function
					1 = 64 bit mode detected
0x94	R/W	[4]	***0****	Audio FIFO Full Interrupt Enable	Audio FIFO Full Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x96	R/W	[4]	***0****	Audio FIFO Full Interrupt	Audio FIFO Full Interrupt 0 = no interrupt detected 1 = interrupt detected

4.4.1.1 Inter-IC Sound (I2S) Audio

The ADV7511 can accommodate from two to eight channels of Inter-IC Sound (I2S) audio at up to a 192KHz sampling rate. The number of channels can be selected in register 0x73[2:0] Which I2S channels are active can be selected in register 0x0C[5:2] If all eight channels (I2S0 – I2S3) are required, setting all bits in registers 0x73[2:0] and 0x0C[5:2] to 1 will select eight channels. If I2S0 only is needed, setting the Channel Count register (0x73[2:0]) and I2S enable (0x0C[2]) to 1 will select this. The I2S Sampling Frequency (0x15[7:4]) must be set appropriately. This value is used along with the VIC to determine pixel repeat (see ► 4.3.4) and sent across the TMDS link in the channel status information contained in the Audio Sample Packet.

The placement of I2S channels into the Audio Sample Packet Subpackets, defined in the ▹ HDMI specification, can be specified in registers 0x0E – 0x11. Default settings place all channels in their respective position (I2S0 left channel in channel 0 left position, I2S3 right channel in channel 3 right position), but this mapping is completely programmable if desired.

The ADV7511 supports standard I2S, left-justified, right-justified, and direct AES3 stream formats via register 0x0C[1:0] and sample word lengths between 16 bits and 24 bits (0x14[3:0]). The ADV7511 supports both 64-bit and 32-bit modes, so either 64 or 32 SCLK edges per channel are valid. The ADV7511 will adapt to 32 or 64 bit mode automatically, and the current mode can be read in register 0x42[3]. See ► Figure 15– ► Figure 20 for I2S format details.

In the direct AES3 stream I2S format, the user can send an IEC60958 sub-frame, seen in ► Figure 13. The data should be aligned as seen in ► Figure 18, with the Preamble left out as shown in ► Figure 14. Notice that the parity bit is replaced by the block start flag. The parity bit will be calculated automatically. The information contained in "C" of I2S0 is used in the HDMI audio sample packet. This information can either be extracted from the stream or programmed through the ADV7511 register map. To choose the channel status source, use register 0x0C[6]. When Channel Status Override (0x0C[6]) is set to extract channel status information from the register map, by setting Audio Sampling Frequency Select (0x0C[7]) to 1, all of the data from the stream will be used except the sampling frequency will be obtained through the Sampling Frequency register (0x15[7:4]). When Audio Sampling Frequency Select is set to 1, the sampling frequency from the register map will be used for pixel repetition decisions as well.

Figure 13 IEC60958 Sub-Frame

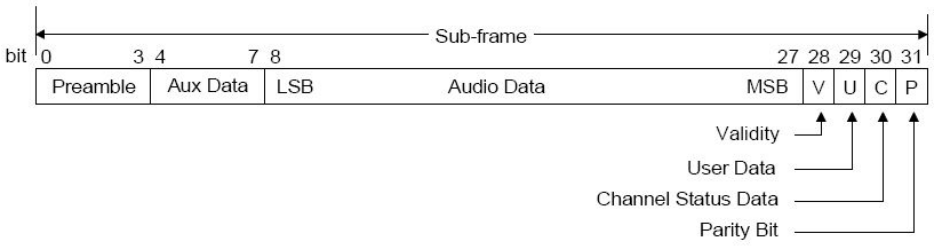


Figure 14 Sub-Frame Format for ADV7511

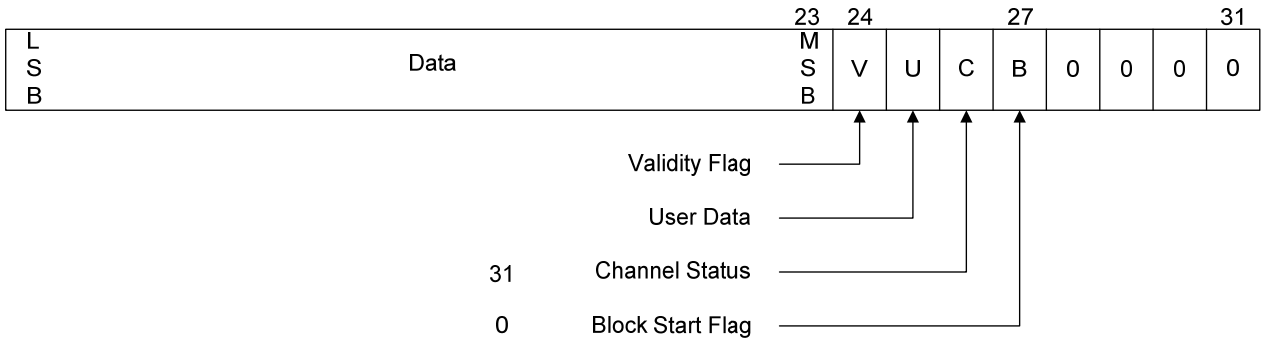


Figure 15 Standard I2S Timing

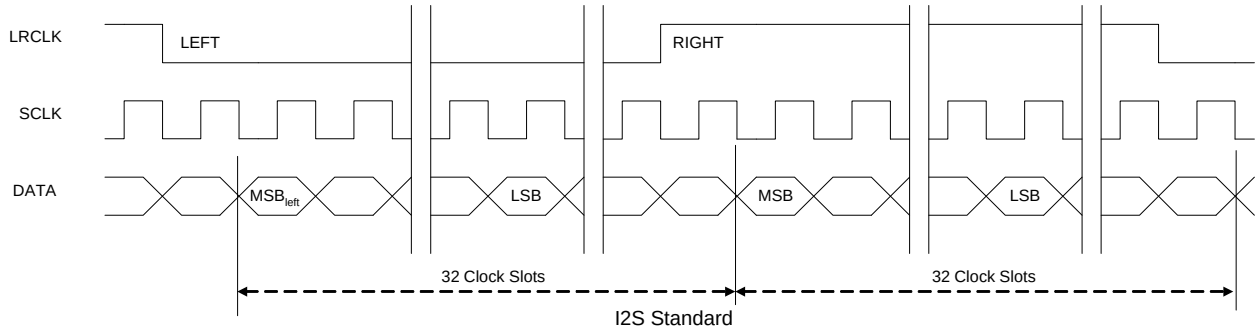


Figure 16 Right-Justified Timing

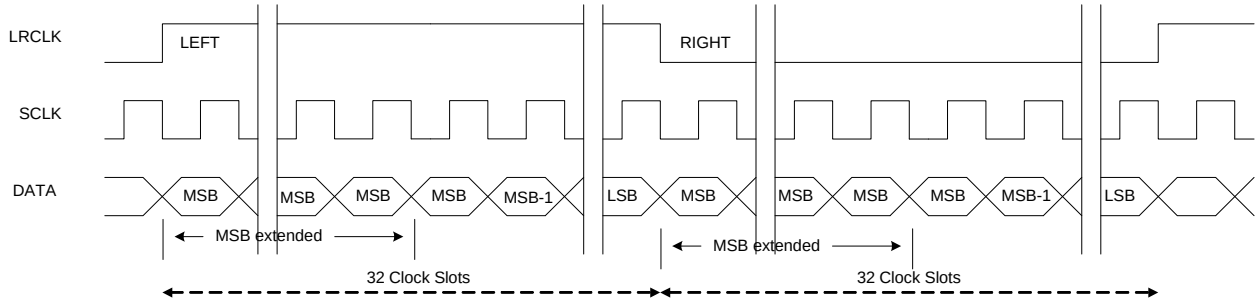
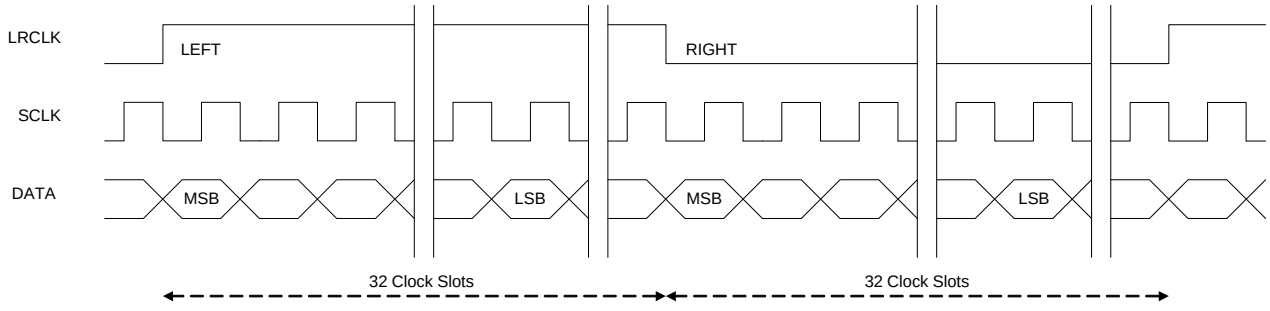


Figure 17 Left-Justified Timing



Serial Audio
Left Justified
R0x0C[1:0] = '10'

Figure 18 AES3 Direct Timing

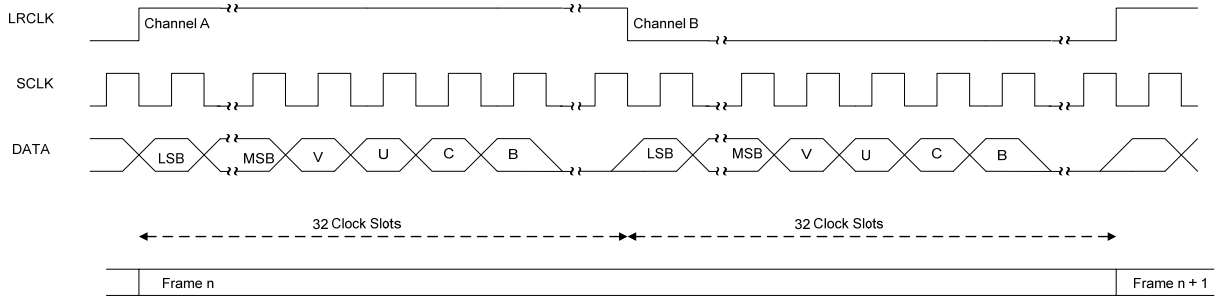
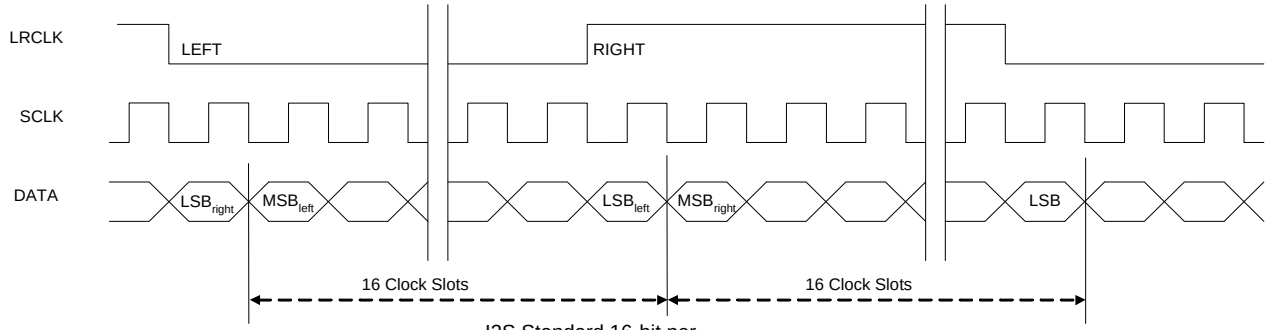


Figure 19 I2S 32 Bit Mode Timing



I2S Standard 16-bit per channel
R0x0C[1:0] = '00'

Figure 20 32 Bit Mode Left- or Right-Justified Timing

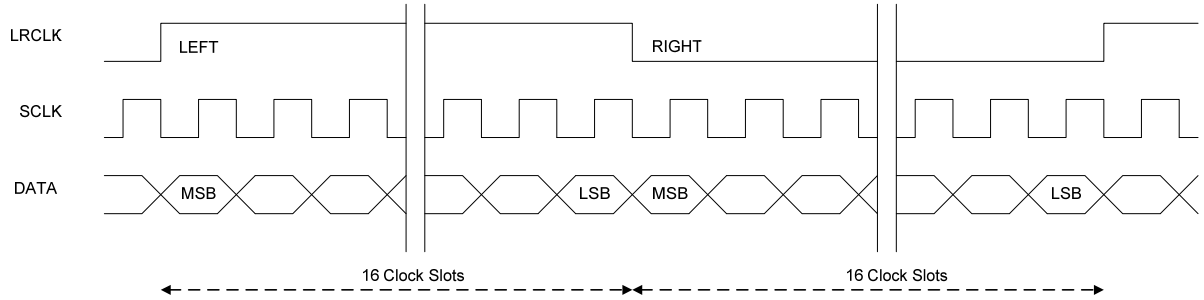


Table 75 Inter-IC Sound (I2S) Audio Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x0A	R/W	[6:4]	*000****	Audio Select	Audio Select All others invalid 000 = I2S 001 = SPDIF 010 = One Bit Audio (DSD) 011 = High Bit Rate (HBR Audio) 100 = DST 101 = N/A 110 = N/A 111 = N/A
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select Case 1: DSD (Audio Select register bits (0x0A[6:4] = 0b010)) 0X = DSD raw mode 1X = SDIF-3 mode Case 2: HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding Case 3: DST (Audio Select register bits (0x0A[6:4] = 0b100)) X0 = normal mode 01 = 2x clock 11 = 1x clock or DDR case 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding

4.4.1.2 Sony/Philips Digital Interface (SPDIF) Audio

The ADV7511 is capable of accepting two-channel LPCM and encoded multi-channel audio up to a 192KHz sampling rate via the Sony/Philips Digital Interface (SPDIF). The detected sampling frequency for SPDIF (from 32KHz to 192KHz) can be read in register0x04[7:4]. For SPDIF, by setting the Audio Frequency Select register (0x0C[7]) to 1, the sampling frequency used to determine pixel repeat can be obtained by the Sampling Frequency register (0x15[7:4]) instead of extracted from the stream; however the sampling frequency read in the SPDIF Sampling Frequency register (0x04) will be sent in the audio sample packet channel status. The ADV7511 is capable of accepting SPDIF with or without an MCLK input. When no MCLK is present, the ADV7511 uses MCLK to internally generate the MCLK and determine the CTS value.

Table 76 Sony/Philips Digital Interface (SPDIF) Audio Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x0A	R/W	[6:4]	*000****	Audio Select	Audio Select All others invalid 000 = I2S 001 = SPDIF 010 = One Bit Audio (DSD) 011 = High Bit Rate (HBR Audio) 100 = DST 101 = N/A 110 = N/A 111 = N/A
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select Case 1: DSD (Audio Select register bits (0x0A[6:4] = 0b010)) 0X = DSD raw mode 1X = SDIF-3 mode Case 2: HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding Case 3: DST (Audio Select register bits (0x0A[6:4] = 0b100)) X0 = normal mode 01 = 2x clock 11 = 1x clock or DDR case 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding

4.4.1.3 Direct Stream Digital (DSD) Audio

Direct Stream Digital (DSD) Audio uses the One Bit Audio packets to transfer data across the TMDS link. Up to eight channels of DSD data can be input onto eight data lines clocked by the DSD_CLK. DSD can be selected as the input format using the Audio Select register (0x0A[6:4]) = 0b010. Raw mode or SDIF-3 mode can be selected by the Audio Mode register (0x0A[3]). Each input can be enabled or disabled in the DSD Enable register (0x46). ► Table 73 shows the register settings for different modes.

For DSD, the Sampling Frequency (Audio InfoFrame) register (0x74[4:2]) needs to be set.Manual pixel repeat mode should be used for DSD as described in Section► 4.3.4.The DSD clock and data are 64 times the corresponding PCM sampling frequencies.

Table 77 Direct Stream Digital (DSD) Audio Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x0A	R/W	[6:4]	*000****	Audio Select	Audio Select All others invalid 000 = I2S 001 = SPDIF 010 = One Bit Audio (DSD) 011 = High Bit Rate (HBR Audio) 100 = DST 101 = N/A 110 = N/A 111 = N/A
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select Case 1: DSD (Audio Select register bits (0x0A[6:4] = 0b010)) 0X = DSD raw mode 1X = SDIF-3 mode Case 2: HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding Case 3: DST (Audio Select register bits (0x0A[6:4] = 0b100)) X0 = normal mode 01 = 2x clock 11 = 1x clock or DDR case 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding
0x46	R/W	[7:0]	00000000	DSD Enable	DSD Channel Enable Each bit enables one of the 8 DSD audio input channels. Bit 0 enables channel 0, and bit 7 enables channel 7.
0x47	R/W	[7]	0*******	DSD Mux Enable	DSD Mux Enable. User has to set this bit to one to use DSD[7:6]. 0 = Disabled 1 = Enabled

4.4.1.4 High Bit-Rate (HBR) Audio

High Bit-Rate (HBR) audio uses the HBR audio packets to transfer compressed data at rates greater than 6.144Mbps across the TMDS link. HBR Audio can be selected as the input format using the Audio Select register (0x0A[6:4]) = 0b011. The use of four-stream or one-stream encoding can be set in the Audio Mode register (0x0A[3]), and the BPM encoding can be selected or deselected using the Audio mode register (0x0A[2]). ► Table 73 shows the register settings for different modes.

Register 0x47[6] can be toggled from 0 to 1 to synchronize the PaPb syncword, which marks the beginning of a stream repetition, with HDMI HBR subpacket 0. For data bursts with a repetition period, which is a multiple of four frames, the synchronization will persist. If the data burst does not have a repetition period of four frames, setting register 0x47[6] to 1 is not needed, but will not have any negative effects. The transition of the bit from 0 to 1 causes the one-time synchronization, so setting the bit from 1 to 0 will have no effect.

For HBR Audio, the Sampling Frequency register (0x15[7:4]) needs to be set to 0b1001.Manual pixel repeat mode should be used for DSD as described in Section► 4.3.4. An MCLK is always required for the BPM encoding modes.

The mapping from the I2S input channels to the HBR subpackets can be set by registers 0x0E to 0x11. When using an ADI HDMI Rx as the input the default should be used. Since there is no standard for chip to chip HBR transfer, different settings may be required for different chips used as the input.

Table 78 High Bit-Rate (HBR) Audio Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x0A	R/W	[6:4]	*000****	Audio Select	Audio Select All others invalid 000 = I2S 001 = SPDIF 010 = One Bit Audio (DSD) 011 = High Bit Rate (HBR Audio) 100 = DST 101 = N/A 110 = N/A 111 = N/A
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select Case 1: DSD (Audio Select register bits (0x0A[6:4] = 0b010)) 0X = DSD raw mode 1X = SDIF-3 mode Case 2: HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding Case 3: DST (Audio Select register bits (0x0A[6:4] = 0b100)) X0 = normal mode 01 = 2x clock 11 = 1x clock or DDR case 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding
0x15	R/W	[7:4]	0000****	I2S Sampling Frequency (CS bits 27-24)	Sampling frequency for I2S audio. This information is used by both the audio Rx and the pixel repetition. 0000 = 44.1 kHz 0001 = Do not use 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = Do not use 0101 = Do not use 0110 = Do not use 0111 = Do not use 1000 = 88.2 kHz 1001 = HBR Audio 1010 = 96.0 kHz 1011 = Do not use 1100 = 176.4 kHz 1101 = Do not use 1110 = 192.0 kHz 1111 = Do not use
0x47	R/W	[6]	*0******	PaPb Sync	For HBR audio this syncs PaPb with sub packet 0.

4.4.1.5 Direct Stream Transfer (DST) Audio

Direct Stream Transfer (DST) audio is compressed DSD audio. This format is sent in frames which are in time slots equal to 1/75 of a second. The DST audio packets will be used to send the data across the TMDS link. ► Figure 21 shows the method for DST input. DST Audio can be selected as the input format using the Audio Select register (0x0A[6:4]) = 0b100. The Audio Mode register (0x0A[3:2]) selects between normal mode, 2x clock, or 1clock/DDR mode. ► Table 73 shows the register settings for different modes. Manual pixel repeat mode should be used for DSD as described in Section► 4.3.4.

Figure 21 DST Timing

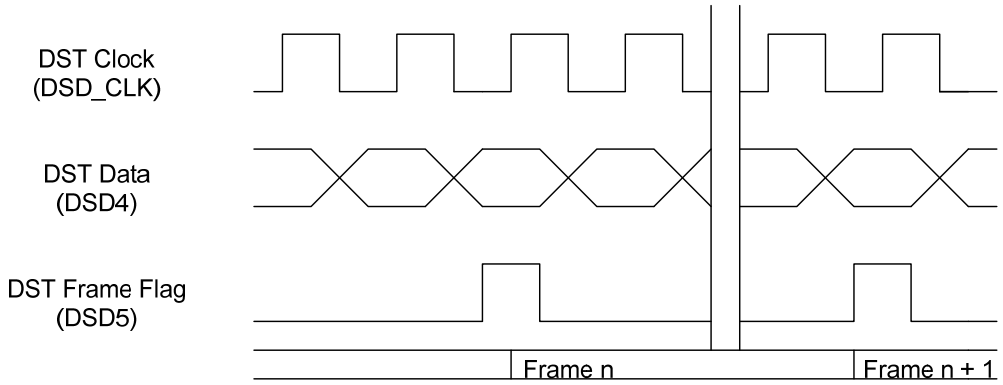


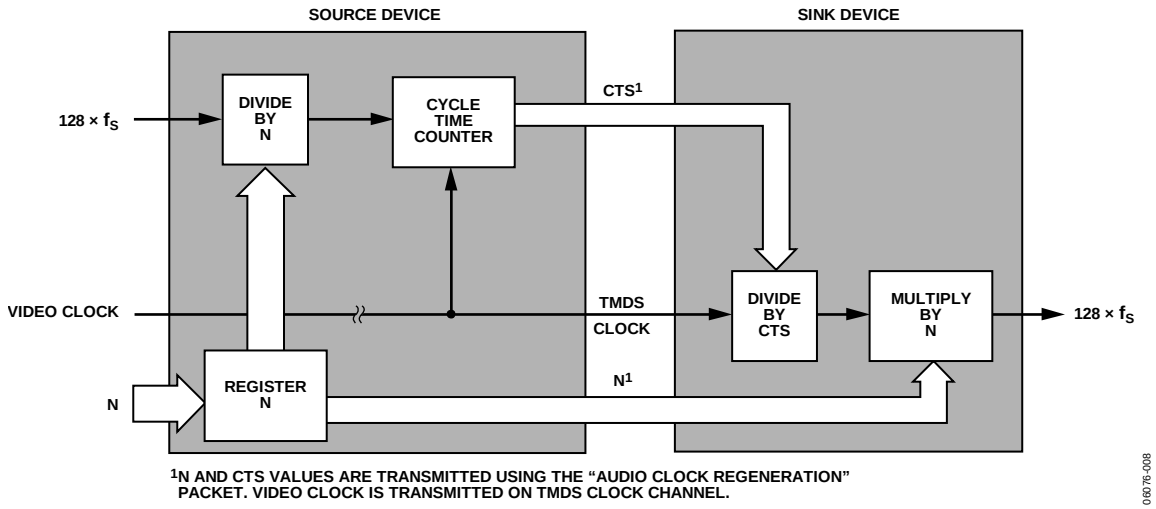
Table 79 Direct Stream Transfer (DST) Audio Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x0A	R/W	[6:4]	*000****	Audio Select	Audio Select All others invalid 000 = I2S 001 = SPDIF 010 = One Bit Audio (DSD) 011 = High Bit Rate (HBR Audio) 100 = DST 101 = N/A 110 = N/A 111 = N/A
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select Case 1: DSD (Audio Select register bits (0x0A[6:4] = 0b010)) 0X = DSD raw mode 1X = SDIF-3 mode Case 2: HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding Case 3: DST (Audio Select register bits (0x0A[6:4] = 0b100)) X0 = normal mode 01 = 2x clock 11 = 1x clock or DDR case 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding

4.4.2 N and CTS

Audio data carried across the HDMI link, which is driven by a TMDS (video) clock only, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration. There are varieties of clock regeneration methods that can be implemented in an HDMI Sink, each with a different set of performance characteristics. The ▹ HDMI specification does not attempt to define exactly how these mechanisms operate. It does, however, present a possible configuration and define the data items that the HDMI Source shall supply to the HDMI Sink in order to allow the HDMI Sink to adequately regenerate the audio clock. It also defines how that data shall be generated. In many video source devices, the audio and video clocks are generated from a common clock (coherent clocks). In this situation, there exists a rational (integer divided by integer) relationship between these two clocks. The HDMI clock regeneration architecture can take advantage of this rational relationship and can also work in an environment where there is no such relationship between these two clocks; that is, where the two clocks are truly asynchronous or where their relationship is unknown.

Figure 22 Audio Clock Regeneration



The Audio Clock Regeneration model in ► Figure 22 illustrates the overall system architecture model used by HDMI for audio clock regeneration. The Source shall determine the fractional relationship between the video clock and an audio reference clock (128*audio sample rate) and shall pass the numerator and denominator for that fraction to the Sink across the HDMI link. The Sink may then recreate the audio clock from the TMDS clock by using a clock divider and a clock multiplier. The exact relationship between the two clocks will be:

$$128\, f_s = f_{TMDS\_CLK}\, \frac{N}{CTS}$$

The Source shall determine the value of the numerator *N* as specified in Section 7.2.1 of the ▹ HDMI specification. Typically, this value *N* will be used in a clock divider to generate an intermediate clock that is slower than the 128*f_S clock by the factor *N*. The Source will typically determine the value of the denominator Cycle Time Stamp (*CTS*) by counting the number of TMDS clocks in each of the 128*f_S/*N* clocks.

4.4.2.1 N Parameter

N shall be an integer number and shall meet the following restriction: $128*f_S/1500\text{Hz} \le N \le 128*f_S/300\text{Hz}$ with a recommended optimal value of $128*f_S/1000\text{Hz}$ approximately equals *N* for coherent audio and video clock Sources. ► Table 80 – Table 82 can be used to determine the value of *N*. For non-coherent sources or sources where coherency is not known, the equations above should be used.

4.4.2.2 CTS Parameter

CTS shall be an integer number that satisfies the following:

$$CTS_{Average} = \frac{f_{TMDS\_CLK} N}{128 f_s}$$

4.4.2.3 Recommended N and Expected CTS Values

The recommended value of *N* for several standard pixel clocks are given in ► Table 80 – Table 82. It is recommended that Sources with non-coherent clocks use the values listed for a pixel clock of "Other."

The ADV7511 has two modes for CTS generation: manual mode and automatic mode. In manual mode, the user can program the CTS number directly into the chip (0x07–0x09) and select this external mode by setting 0x0A[7] to 1. In automatic mode, the chip computes the CTS based on the actual audio and video rates. This can be selected by setting 0x0A[7] to 0 and the results can be read from 0x04 – 0x06. The manual mode is good for coherent audio and video, where the audio and video clock are generated from the same crystal; thus CTS should be a fixed number. The auto mode is good for incoherent audio -video, where there is no simple integer ratio between the audio and video clock. The 20 bit *N* value can be programmed into the ADV7511 in registers 0x01–0x03.

Table 80 Recommended N and Expected CTS Values for 32KHz Audio

	32KHz	
Pixel Clock (MHz)	**N**	**CTS**
25.2 / 1.001	4576	28125
25.2	4096	25200
27	4096	27000
27 * 1.001	4096	27027
54	4096	54000
54 * 1.001	4096	54054
74.25 / 1.001	11648	210937 – 210938
74.25	4096	74250
148.5 / 1.001	11648	421875
148.5	4096	148500
Other	4096	Measured

Table 81 Recommended N and Expected CTS values for 44.1KHz Audio and Multiples

	44.1KHz		88.2KHz		176.4KHz	
Pixel Clock (MHz)	**N**	**CTS**	**N**	**CTS**	**N**	**CTS**
25.2 / 1.001	7007	31250	14014	31250	28028	31250
25.2	6272	28000	12544	28000	25088	28000
27	6272	30000	12544	30000	25088	30000
27 * 1.001	6272	30030	12544	30030	25088	30030
54	6272	60000	12544	60000	25088	60000
54 * 1.001	6272	60060	12544	60060	25088	60060
74.25 / 1.001	17836	234375	35672	234375	71344	234375
74.25	6272	82500	12544	82500	25088	82500
148.5 / 1.001	8918	234375	17836	234375	35672	234375
148.5	6272	16500	12544	16500	25088	16500
Other	6272	measured	12544	measured	25088	Measured

Table 82 Recommended N and Expected CTS values for 448KHz Audio and Multiples

	48KHz		96KHz		192KHz	
Pixel Clock (MHz)	**N**	**CTS**	**N**	**CTS**	**N**	**CTS**
25.2 / 1.001	6864	28125	13728	28125	27456	28125
25.2	6144	25200	12288	25200	24576	25200
27	6144	27000	12288	27000	24576	27000
27 * 1.001	6144	27027	12288	27027	24576	27027
54	6144	54000	12288	54000	24576	54000
54 * 1.001	6144	54054	12288	54054	24576	54054
74.25 / 1.001	11648	140625	35672	140625	46592	140625
74.25	6144	74250	12288	74250	24576	74250
148.5 / 1.001	5824	140625	17836	140625	23296	140625
148.5	6144	148500	12288	148500	24576	148500
Other	6144	measured	12288	measured	24576	measured

Table 83 N and CTS Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x01	R/W	[19:0]	****0000	N	20 bit N used with CTS to regenerate the audio clock in the receiver.
0x02			00000000		
0x03			00000000		
0x04	RO	[19:0]	****0000	CTS Automatic	Cycle Time Stamp (CTS) Automatically Generated This 20 bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits see 0x05 and 0x06.
0x05			00000000		
0x06			00000000		
0x07	R/W	[19:0]	****0000	CTS Manual	Cycle Time Stamp (CTS) Manually Entered This 20 bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits see 0x08 and 0x09.
0x08			00000000		
0x09			00000000		
0x0A	R/W	[7]	0*******	CTS Select	CTS Source Select. 0 = CTS Automatic 1 = CTS Manual
0x44	R/W	[6]	*1******	N CTS Packet Enable	N CTS Packet Enable 0 = Disabled 1 = Enabled

4.4.3 Audio Sample Packets

By setting the Chanel Count (CC) register (0x73[2:0]) to greater than three channels, the eight-channel audio packet format will be used. The I2S can be routed to different subpackets using registers 0xE – 0x11. The Channel Allocation (CA) register (0x76[7:0]) must be set to a speaker mapping that corresponds to the I2S to subpacket routing. Using SPDIF has a default setting of two channels.

The audio packets in HDMI use the channel status format from IEC60958. When using I2S, the information sent in the channel status fields is provided by registers Copyright Bit (0x12[5]), Pre-emphasis (0x12[4:2]), clock accuracy (0x12[1:0]),

category code (0x13), source number (0x14[7:4]), word length (0x14[3:0]), bits [1:0] 0x12[7:6], and audio sampling frequency (0x15[7:4]). In SPDIF mode the channel status information is taken from the SPDIF stream.

4.4.3.1 Details for I2S Channel Status

► Table 84 shows the ADV7511 register map location or fixed value for each bit in the channel status information sent across the HDMI link. This is applicable for I2S modes 0 – 3 as set in register 0x0C[1:0].

Table 84 I2S Channel Status ADV7511 Register Map Location or Fixed Value

Bit	Name	ADV7511 Register Used to Set Field or Fixed Value
0	consumer use.	0x12[6]
1	audio sample word	0x12[7]
2	copyright	0x12[5]
3	emphasis	0x12[2]
4	emphasis	0x12[3]
5	emphasis	0x12[4]
6	mode	0
7	mode	0
8	category code	0x13[0]
9	category code	0x13[1]
10	category code	0x13[2]
11	category code	0x13[3]
12	category code	0x13[4]
13	category code	0x13[5]
14	category code	0x13[6]
15	category code	0x13[7]
16	source number	0x14[4]
17	source number	0x14[5]
18	source number	0x14[6]
19	source number	0x14[7]
20	channel number	See ▶ Figure 23
21	channel number	See ▶ Figure 23
22	channel number	See ▶ Figure 23
23	channel number	See ▶ Figure 23
24	sampling frequency	0x15[4]
25	sampling frequency	0x15[5]
26	sampling frequency	0x15[6]
27	sampling frequency	0x15[7]
28	clock accuracy	0x12[0]
29	clock accuracy	0x12[1]
30	Not Defined	0
31	Not Defined	0
32	word length	0x14[0]
33	word length	0x14[1]
34	word length	0x14[2]
35	word length	0x14[3]
36	original sampling frequency	0
37	original sampling frequency	0
38	original sampling frequency	0
39	original sampling frequency	0
40	CGMS-A	0
41	CGMS-A	0
42	Not Defined	0
191	Not Defined	0

In ► Figure 23 the layout bit in the Audio Sample Packet Header and the sample_present.spX bit are determined based on the Audio InfoFrame Channel Count register (0x73[2:0]). For example, if Channel Count = 0b001, indicating stereo audio, the layout bit will be zero and all Audio Sample Subpackets will contain information for channel 1 and 2. If Channel Count = 0b011, indicating four channels, the layout bit will be one, and sample_present.sp0 = 1, sample_present.sp1 = 1, sample_present.sp2 = 0, and sample_present.sp2 = 0. ► Figure 23 shows how the channel number bits will be set based on the layout bit and sample_present.spX.

Figure 23 Definition of Channel Status Bits 20 to 23

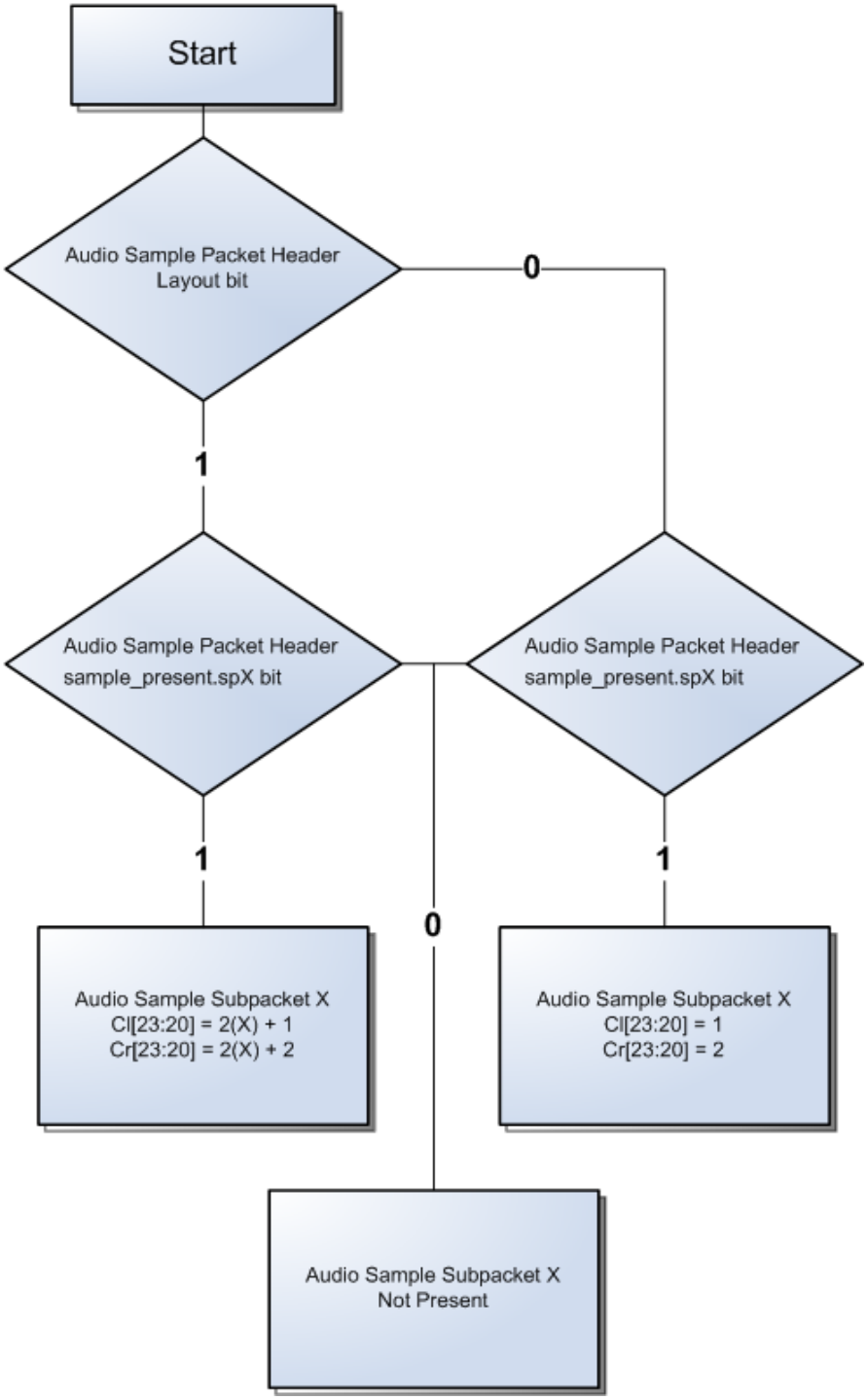


Table 85 Audio Sample Packets Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x0E	R/W	[5:3]	**000***	Subpacket 0 L Source	Source of sub packet 0, left channel
		[2:0]	*****001	Subpacket 0 R Source	Source of sub packet 0, right channel
0x0F	R/W	[5:3]	**010***	Subpacket 1 L Source	Source of sub packet 1, left channel
		[2:0]	*****011	Subpacket 1 R Source	Source of sub packet 1, right channel
0x10	R/W	[5:3]	**100***	Subpacket 2 L Source	Source of sub packet 2, left channel
		[2:0]	*****101	Subpacket 2 R Source	Source of sub packet 2, right channel
0x11	R/W	[5:3]	**110***	Subpacket 3 L Source	Source of sub packet 3, left channel
		[2:0]	*****111	Subpacket 3 R Source	Source of sub packet 3, right channel
0x12	R/W	[7]	0*******	Audio Sample Word (CS bit 1)	Audio Sample Word 0 = Audio sample word represents linear PCM samples 1 = Audio sample word used for other purposes Consumer Use Should be 0 for HDMI
		[6]	*0******	Consumer Use (CS bit 0)	Consumer Use Bit 0 = Audio sample word represents linear PCM samples 1 = Audio sample word used for other purposes
		[5]	**0*****	Copyright Bit (CS bit 2)	Copy Right Bit 0 = Copyright Protected 1 = Not Copyright Protected
		[4:2]	***000**	Additional Audio Info (CS bits 5-3)	Additional information for Channel Status Bits 000 = 2 audio channels w/o pre-emphasis 001 = 2 audio channels with 50/15uS pre-emphasis 010 = Fixed 011 = Fixed
		[1:0]	******00	Audio Clock Accuracy (CS bits 29-28)	Audio Clock Accuracy 00 = level II - normal accuracy +/-1000 X 10-6 10 = level III -variable pitch shifted clock 01 = level I - high accuracy +/-50 X 10-6 11 = Fixed
0x13	R/W	[7:0]	00000000	Category Code (CS bits 15-8)	Channel Status Category Code
0x14	R/W	[7:4]	0000****	Source Number (CS bits 19-16)	Channel Status Source Number
		[3:0]	****0000	Word Length (CS bits 35-32)	Audio Word Length 0000 = Not Specified 0001 = Not Specified 0010 = 16 Bits 0011 = 20 Bits 0100 = 18 Bits 0101 = 22 Bits 0110 = No description 0111 = No description 1000 = 19 Bits 1001 = 23 Bits 1010 = 20 Bits

Address	Type	Bits	Default Value	Register Name	Function
					1011 = 24 Bits 1100 = 17 Bits 1101 = 21 Bits 1110 = No description 1111 = No description
0x15	R/W	[7:4]	0000****	I2S Sampling Frequency (CS bits 27-24)	Sampling frequency for I2S audio. This information is used by both the audio Rx and the pixel repetition. 0000 = 44.1 kHz 0001 = Do not use 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = Do not use 0101 = Do not use 0110 = Do not use 0111 = Do not use 1000 = 88.2 kHz 1001 = HBR Audio 1010 = 96.0 kHz 1011 = Do not use 1100 = 176.4 kHz 1101 = Do not use 1110 = 192.0 kHz 1111 = Do not use
0x44	R/W	[5]	**1*****	Audio Sample Packet Enable	Audio Sample Packet Enable 0 = Disabled 1 = Enabled
0x47	R/W	[5]	**0*****	Audio Sample 3 Valid	Indicates when sub packet 3 has invalid data.
		[4]	***0****	Audio Sample 2 Valid	Indicates when sub packet 2 has invalid data.
		[3]	****0***	Audio Sample 1 Valid	Indicates when sub packet 1 has invalid data.
		[2]	*****0**	Audio Sample 0 Valid	Indicates when sub packet 0 has invalid data.

4.4.4 Audio InfoFrame

The audio InfoFrame allows the receiver to identify the characteristics of an audio stream before the channel status information is available. The Audio Channel Count register (0x73[2:0]) sets the channel count field for the InfoFrame, and determines the number of channels to send in the audio sample packets. Down Mix Inhibit (0x77[7]), Level Shift Values (0x77[6:3]), and Speaker Mapping (0x76) are defined in the ▹ *CEA-861D* specification. The number of channels in the Channel Count register must match the number of channels in the Speaker Mapping register. The values for the Speaker Mapping bits are included in ► Table 86 for reference.

To avoid a partial update of the Audio InfoFrame Packets the Packet Update feature should be used. By setting the Audio InfoFrame Packet Update register bit to '1', the current values will be stored and sent in the packets. The user should update the values then set the Audio InfoFrame Packet Update register bit to 0 to begin sending the new packets. See section 4.2.5 for details.

Table 86 Audio Channel Mapping

CA (Speaker Mapping)					Channel Number[2]							
4	3	2	1	0	8	7	6	5	4	3	2	1
0	0	0	0	0					-	-	FR	FL
0	0	0	0	1					-	LFE	FR	FL
0	0	0	1	0					FC	-	FR	FL
0	0	0	1	1					FC	LFE	FR	FL
0	0	1	0	0				RC	-	-	FR	FL
0	0	1	0	1				RC	-	LFE	FR	FL
0	0	1	1	0				RC	FC	-	FR	FL
0	0	1	1	1				RC	FC	LFE	FR	FL
0	1	0	0	0			RR	RL	-	-	FR	FL
0	1	0	0	1			RR	RL	-	LFE	FR	FL
0	1	0	1	0			RR	RL	FC	-	FR	FL
0	1	0	1	1	-	-	RR	RL	FC	LFE	FR	FL
0	1	1	0	0	-	RC	RR	RL	-	-	FR	FL
0	1	1	0	1	-	RC	RR	RL	-	LFE	FR	FL
0	1	1	1	0	-	RC	RR	RL	FC	-	FR	FL
0	1	1	1	1	-	RC	RR	RL	FC	LFE	FR	FL
1	0	0	0	0	RRC	RLC	RR	RL	-	-	FR	FL
1	0	0	0	1	RRC	RLC	RR	RL	-	LFE	FR	FL
1	0	0	1	0	RRC	RLC	RR	RL	FC	-	FR	FL
1	0	0	1	1	RRC	RLC	RR	RL	FC	LFE	FR	FL
1	0	1	0	0	FRC	FLC	-	-	-	-	FR	FL
1	0	1	0	1	FRC	FLC	-	-	-	LFE	FR	FL
1	0	1	1	0	FRC	FLC	-	-	FC	-	FR	FL
1	0	1	1	1	FRC	FLC	-	-	FC	LFE	FR	FL
1	1	0	0	0	FRC	FLC	-	RC	-	-	FR	FL
1	1	0	0	1	FRC	FLC	-	RC	-	LFE	FR	FL
1	1	0	1	0	FRC	FLC	-	RC	FC	-	FR	FL
1	1	0	1	1	FRC	FLC	-	RC	FC	LFE	FR	FL
1	1	1	0	0	FRC	FLC	RR	RL	-	-	FR	FL
1	1	1	0	1	FRC	FLC	RR	RL	-	LFE	FR	FL
1	1	1	1	0	FRC	FLC	RR	RL	FC	-	FR	FL
1	1	1	1	1	FRC	FLC	RR	RL	FC	LFE	FR	FL

Table 87 Audio InfoFrame Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x44	R/W	[3]	****1***	Audio InfoFrame Enable	Audio InfoFrame Enable 0 = Disabled 1 = Enabled
0x4A	R/W	[7]	1*******	Auto Checksum Enable	Auto Checksum Enable 0 = Use checksum from registers 1 = Use automatically generated checksum
		[5]	**0*****	Audio InfoFrame Packet Update	Audio InfoFrame Packet Update: Before updating the Audio InfoFrame Packet using I2C set to '1' to continue sending the current values.

[2] FL = Front Left, FC = FrontCenter, FR = Front Right, FLC = FrontLeftCenter, FRC = FrontRightCenter, RL = Rear Left, RC = RearCenter, RR = Rear Right, RLC = RearLeftCenter, RRC = RearRightCenter, LFE = Low Frequency Effect

Address	Type	Bits	Default Value	Register Name	Function
					0 = Audio InfoFrame Packet I2C update inactive 1 = Audio InfoFrame Packet I2C update active
0x74	R/W	[7:5]	000*****	Byte 2 bit [7:5] (Audio InfoFrame)	Fixed per HDMI spec. Set to 0.
		[4:2]	***000**	Sampling Frequency (Audio InfoFrame)	Audio sampling frequency. Should be 0, except for SACD.
		[1:0]	******00	Sample Size (Audio InfoFrame)	Set to 0
0x75	R/W	[7:0]	00000000	Byte 3 (Audio InfoFrame)	Set to 0
0x76	R/W	[7:0]	00000000	Speaker Mapping (Audio InfoFrame)	CA[7:0] Speaker mapping or placement for up to 2 channels.
0x77	R/W	[7]	0*******	DM_INH (Audio InfoFrame)	Down-mix Inhibit
		[6:3]	*0000***	Level Shift (Audio InfoFrame)	LSV[3:0]-Audio Level Shift Values With Attenuation Information 0000 = 0dB attenuation 0001 = 1dB attenuation 0010 = 2dB attenuation 0011 = 3dB attenuation 0100 = 4dB attenuation 0101 = 5dB attenuation 0110 = 6dB attenuation 0111 = 7dB attenuation 1000 = 8dB attenuation 1001 = 9dB attenuation 1010 = 10dB attenuation 1011 = 11dB attenuation 1100 = 12dB attenuation 1101 = 13dB attenuation 1110 = 14dB attenuation 1111 = 15dB attenuation
		[2]	*****0**	Byte 5 bit [2]	Fixed per HDMI spec
		[1:0]	******00	LFEPBL[1:0]	Set to 0b0,ow Frequency Effect Playback Level 00 = No information 01 = 0 dB playback 10 = +10 dB playback 11 = Reserved
0x78	R/W	[7:0]	00000000	Byte 6 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x79	R/W	[7:0]	00000000	Byte 7 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x7A	R/W	[7:0]	00000000	Byte 8 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x7B	R/W	[7:0]	00000000	Byte 9 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'
0x7C	R/W	[7:0]	00000000	Byte 10 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'

4.4.5 Audio Content Protection (ACP) Packet

The Audio Content Protection (ACP) packet is used for transmitting content-related information about the active audio stream. Use of the ACP will be defined in the license agreements of the protected audio stream.

To avoid a partial update of the ACP Packets the Packet Update features should be used. By setting the ACP Packet Update register bit to '1', the current values will be stored and sent in the packets. The user should update the values then set the ACP Packet Update register bit to '0' to begin sending the new packets. See section 4.2.5 for details.

Table 88 Audio Content Protection (ACP) Packet Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[4]	***0****	ACP Packet Enable	ACP Packet Enable 0 = Disabled 1 = Enabled

Table 89 **Audio Content Protection (ACP) Packet Related Registers (Packetmemory Map)**

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[7:0]	00000000	ACP Header Byte 0	
0x41	R/W	[7:0]	00000000	ACP Header Byte 1	
0x42	R/W	[7:0]	00000000	ACP Header Byte 2	
0x43	R/W	[7:0]	00000000	ACP Packet Byte 0	
0x44	R/W	[7:0]	00000000	ACP Packet Byte 1	
0x45	R/W	[7:0]	00000000	ACP Packet Byte 2	
0x46	R/W	[7:0]	00000000	ACP Packet Byte 3	
0x47	R/W	[7:0]	00000000	ACP Packet Byte 4	
0x48	R/W	[7:0]	00000000	ACP Packet Byte 5	
0x49	R/W	[7:0]	00000000	ACP Packet Byte 6	
0x4A	R/W	[7:0]	00000000	ACP Packet Byte 7	
0x4B	R/W	[7:0]	00000000	ACP Packet Byte 8	
0x4C	R/W	[7:0]	00000000	ACP Packet Byte 9	
0x4D	R/W	[7:0]	00000000	ACP Packet Byte 10	
0x4E	R/W	[7:0]	00000000	ACP Packet Byte 11	
0x4F	R/W	[7:0]	00000000	ACP Packet Byte 12	
0x50	R/W	[7:0]	00000000	ACP Packet Byte 13	
0x51	R/W	[7:0]	00000000	ACP Packet Byte 14	
0x52	R/W	[7:0]	00000000	ACP Packet Byte 15	
0x53	R/W	[7:0]	00000000	ACP Packet Byte 16	
0x54	R/W	[7:0]	00000000	ACP Packet Byte 17	
0x55	R/W	[7:0]	00000000	ACP Packet Byte 18	
0x56	R/W	[7:0]	00000000	ACP Packet Byte 19	
0x57	R/W	[7:0]	00000000	ACP Packet Byte 20	
0x58	R/W	[7:0]	00000000	ACP Packet Byte 21	
0x59	R/W	[7:0]	00000000	ACP Packet Byte 22	
0x5A	R/W	[7:0]	00000000	ACP Packet Byte 23	
0x5B	R/W	[7:0]	00000000	ACP Packet Byte 24	
0x5C	R/W	[7:0]	00000000	ACP Packet Byte 25	

Address	Type	Bits	Default Value	Register Name	Function
0x5D	R/W	[7:0]	00000000	ACP Packet Byte 26	
0x5E	R/W	[7:0]	00000000	ACP Packet Byte 27	
0x5F	R/W	[7]	0*******	ACP Packet Update	ACP Packet Update: Before updating the ACP Packet using I2C set to '1' to continue sending the current values. 0 = ACP Packet I2C update inactive 1 = ACP Packet I2C update active.

4.4.6 International Standard Recording Code (ISRC) Packet

If the Supports_AI bit in the Vendor Specific Data Block (VSDB) of the sink EDID is 1 then the International Standard Recording Code (ISRC) packets 1 and 2 can be transmitted. The use of the ISRC fields is described in ▹ "DVD Specifications for Read-Only Disc", Part 4: AUDIO SPECIFICATIONS Version 1.0, March 1999, Annex B.

To avoid a partial update of the ISRC Packets the Packet Update features should be used. By setting the ISRC1 Packet Update or ISRC2 Packet Update register bit to 1 the current values will be stored and sent in the packets. The user should update the values then set the ISRC1 Packet Update or ISRC2 Packet Update register bit to 0 to begin sending the new packets. See section 4.2.5 for details.

Table 90 International Standard Recording Code (ISRC) Packet Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x40	R/W	[3]	****0***	ISRC Packet Enable	ISRC Packet Enable 0 = Disabled 1 = Enabled

Table 91 International Standard Recording Code (ISRC) Packet Related Registers (Packetmemory Map)

Address	Type	Bits	Default Value	Register Name	Function
0x60	R/W	[7:0]	00000000	ISRC1 Header Byte 0	
0x61	R/W	[7:0]	00000000	ISRC1 Header Byte 1	
0x62	R/W	[7:0]	00000000	ISRC1 Header Byte 2	
0x63	R/W	[7:0]	00000000	ISRC1 Packet Byte 0	
0x64	R/W	[7:0]	00000000	ISRC1 Packet Byte 1	
0x65	R/W	[7:0]	00000000	ISRC1 Packet Byte 2	
0x66	R/W	[7:0]	00000000	ISRC1 Packet Byte 3	
0x67	R/W	[7:0]	00000000	ISRC1 Packet Byte 4	
0x68	R/W	[7:0]	00000000	ISRC1 Packet Byte 5	
0x69	R/W	[7:0]	00000000	ISRC1 Packet Byte 6	

Address	Type	Bits	Default Value	Register Name	Function
0x6A	R/W	[7:0]	00000000	ISRC1 Packet Byte 7	
0x6B	R/W	[7:0]	00000000	ISRC1 Packet Byte 8	
0x6C	R/W	[7:0]	00000000	ISRC1 Packet Byte 9	
0x6D	R/W	[7:0]	00000000	ISRC1 Packet Byte 10	
0x6E	R/W	[7:0]	00000000	ISRC1 Packet Byte 11	
0x6F	R/W	[7:0]	00000000	ISRC1 Packet Byte 12	
0x70	RO	[7:0]	00000000	ISRC1 Packet Byte 13	
0x71	RO	[7:0]	00000000	ISRC1 Packet Byte 14	
0x72	RO	[7:0]	00000000	ISRC1 Packet Byte 15	
0x73	RO	[7:0]	00000000	ISRC1 Packet Byte 16	
0x74	RO	[7:0]	00000000	ISRC1 Packet Byte 17	
0x75	R/W	[7:0]	00000000	ISRC1 Packet Byte 18	
0x76	R/W	[7:0]	00000000	ISRC1 Packet Byte 19	
0x77	R/W	[7:0]	00000000	ISRC1 Packet Byte 20	
0x78	R/W	[7:0]	00000000	ISRC1 Packet Byte 21	
0x79	R/W	[7:0]	00000000	ISRC1 Packet Byte 22	
0x7A	R/W	[7:0]	00000000	ISRC1 Packet Byte 23	
0x7B	R/W	[7:0]	00000000	ISRC1 Packet Byte 24	
0x7C	R/W	[7:0]	00000000	ISRC1 Packet Byte 25	
0x7D	R/W	[7:0]	00000000	ISRC1 Packet Byte 26	
0x7E	R/W	[7:0]	00000000	ISRC1 Packet Byte 27	
0x7F	R/W	[7]	0*******	ISRC1 Packet Update	ISRC1 Packet Update: Before updating the ISRC1 Packet using I2C set to '1' to continue sending the current values. 0 = ISRC1 Packet I2C update inactive 1 = ISRC1 Packet I2C update active
0x80	R/W	[7:0]	00000000	ISRC2 Header Byte 0	
0x81	R/W	[7:0]	00000000	ISRC2 Header Byte 1	
0x82	R/W	[7:0]	00000000	ISRC2 Header Byte 2	
0x83	R/W	[7:0]	00000000	ISRC2 Packet Byte 0	
0x84	R/W	[7:0]	00000000	ISRC2 Packet Byte 1	
0x85	R/W	[7:0]	00000000	ISRC2 Packet Byte 2	

Address	Type	Bits	Default Value	Register Name	Function
0x86	R/W	[7:0]	00000000	ISRC2 Packet Byte 3	
0x87	R/W	[7:0]	00000000	ISRC2 Packet Byte 4	
0x88	R/W	[7:0]	00000000	ISRC2 Packet Byte 5	
0x89	R/W	[7:0]	00000000	ISRC2 Packet Byte 6	
0x8A	R/W	[7:0]	00000000	ISRC2 Packet Byte 7	
0x8B	R/W	[7:0]	00000000	ISRC2 Packet Byte 8	
0x8C	R/W	[7:0]	00000000	ISRC2 Packet Byte 9	
0x8D	R/W	[7:0]	00000000	ISRC2 Packet Byte 10	
0x8E	R/W	[7:0]	00000000	ISRC2 Packet Byte 11	
0x8F	R/W	[7:0]	00000000	ISRC2 Packet Byte 12	
0x90	R/W	[7:0]	00000000	ISRC2 Packet Byte 13	
0x91	R/W	[7:0]	00000000	ISRC2 Packet Byte 14	
0x92	R/W	[7:0]	00000000	ISRC2 Packet Byte 15	
0x93	R/W	[7:0]	00000000	ISRC2 Packet Byte 16	
0x94	R/W	[7:0]	00000000	ISRC2 Packet Byte 17	
0x95	R/W	[7:0]	00000000	ISRC2 Packet Byte 18	
0x96	R/W	[7:0]	00000000	ISRC2 Packet Byte 19	
0x97	R/W	[7:0]	00000000	ISRC2 Packet Byte 20	
0x98	R/W	[7:0]	00000000	ISRC2 Packet Byte 21	
0x99	R/W	[7:0]	00000000	ISRC2 Packet Byte 22	
0x9A	R/W	[7:0]	00000000	ISRC2 Packet Byte 23	
0x9B	R/W	[7:0]	00000000	ISRC2 Packet Byte 24	
0x9C	R/W	[7:0]	00000000	ISRC2 Packet Byte 25	
0x9D	R/W	[7:0]	00000000	ISRC2 Packet Byte 26	
0x9E	R/W	[7:0]	00000000	ISRC2 Packet Byte 27	
0x9F	R/W	[7]	0*******	ISRC2 Packet Update	ISRC2 Packet Update: Before updating the ISRC2 Packet using I2C set to '1' to continue sending the current values. 0 = ISRC2 Packet I2C update inactive 1 = ISRC2 Packet I2C update active

4.5 Audio Return Channel (ARC)

One of the HDMI v1.4 features that has been incorporated in the ADV7511 is the Audio Return Channel portion of HEAC . With this capability, the TV can send back audio to the TMDS source for processing and distribution. This audio channel can be sent over a differential pair (common mode component) or on a single line. The common mode signals are on the HEAC+ pin and the HEAC- pin. A single mode transmission will be on the HEAC+ pin. The ARC allows audio from a display with a tuner to be sent to a receiver over the HDMI cable for better audio reproduction. All HDMI cables will support this feature and use of this can reduce the amount of cables in the system.

The audio data is a stereo L-PCM (IEC 60958-1) stream supporting 32KHz, 44.1KHz or 48KHz sampling rates. These represent a clock rate of respectively: 4.096MHz, 5.6448MHz and 6.144MHz. Compressed audio as described in IEC 61937 is optional.

Control of the ARC is initiated by the sink over the CEC lines. The capabilities of the source can be discovered in this fashion whenthe TMDS sink initiates the use of the ARC line(s).

4.5.1 ARC Configuration

The ADV7511's ARC receiver accepts single-ended or common mode signals and directs the resulting SPDIF signal to the SPDIF_OUT pin. A block diagram of the ADV7511's ARC circuit is illustrated in ►Figure 24.To initialize and power on the ARC circuit, the following register bits must be set:

- Select Single ended or common mode by setting 0xDF[7] to '0' or '1'
- Set "ARC Disable bit 0xDF[0] to '0'

When ARC is not being used, the ARC Disable bit (0xDF[0]) should be set to its default value of '1'. The ARC receiver control registers are shown in ►Table 92.

Figure 24 ARC Hardware Configuration

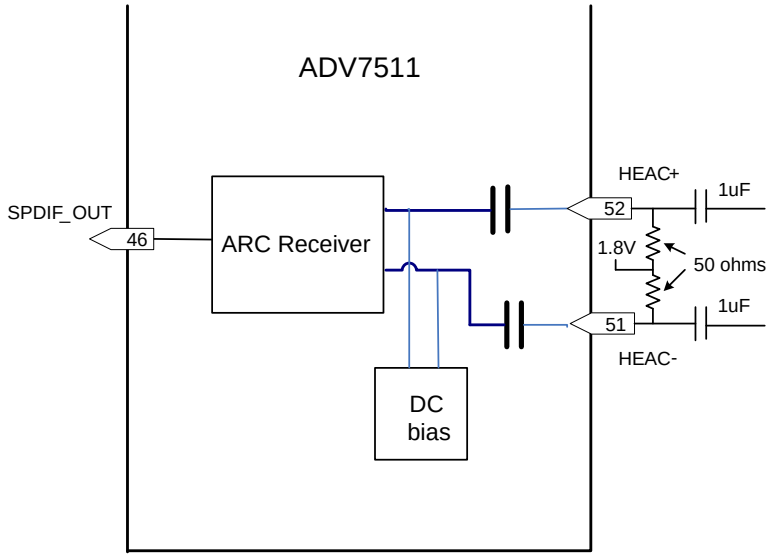


Table 92 Audio Return Channel (ARC) Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0xDF	R/W	[7]	0*******	ARC Mode Select	ARC Single Ended or Common Mode Selection, ARC Disable 0 = Common Mode ARC Input 1 = Single Ended ARC Input
		[0]	*******1	ARC Power Down Control	ARC Power Down Control 0 = ARC Powered up 1 = ARC in Power Down

4.6 EDID Handling

The ADV7511 has an I2C master (DDCSDA and DDCSCL) to read the EDID. It begins buffering segment 0 of the Sink's EDID after HPD is detected and ADV7511 is powered up. The system can request additional segments by programming the EDID Segment register (0xC4). An interrupt bit 0x96[2] indicates that a 256-byte EDID read has been completed, and the information is available in the EDID Memory. The EDID Memory is at I2C address 0x7E by default. This is the default address but can be changed by writing the desired address into the EDID Memory Address register (0x43 of the main register map).

4.6.1.1 EDID Definitions

EnhancedEDID (E-EDID) supports up to 256 segments. A segment is a 256-byte segment of EDID containing information for either one or two 128-byte EDID blocks. A typical HDMI system will have only two EDID blocks and will only use segment 0. The first EDID block is always a base EDID structure defined in VESA EDID specifications; the second EDID block is usually the CEA extension defined in the ▹ *CEA-861D specification*.

EDID and HDCP use a shared memory space. During HDCP repeater initialization, the EDID data is overwritten with HDCP information. EDID is not re-read after HDCP initialization. If the user would like to re-buffer an EDID segment the EDID re-read register described in section 4.6.1.4 should be used.

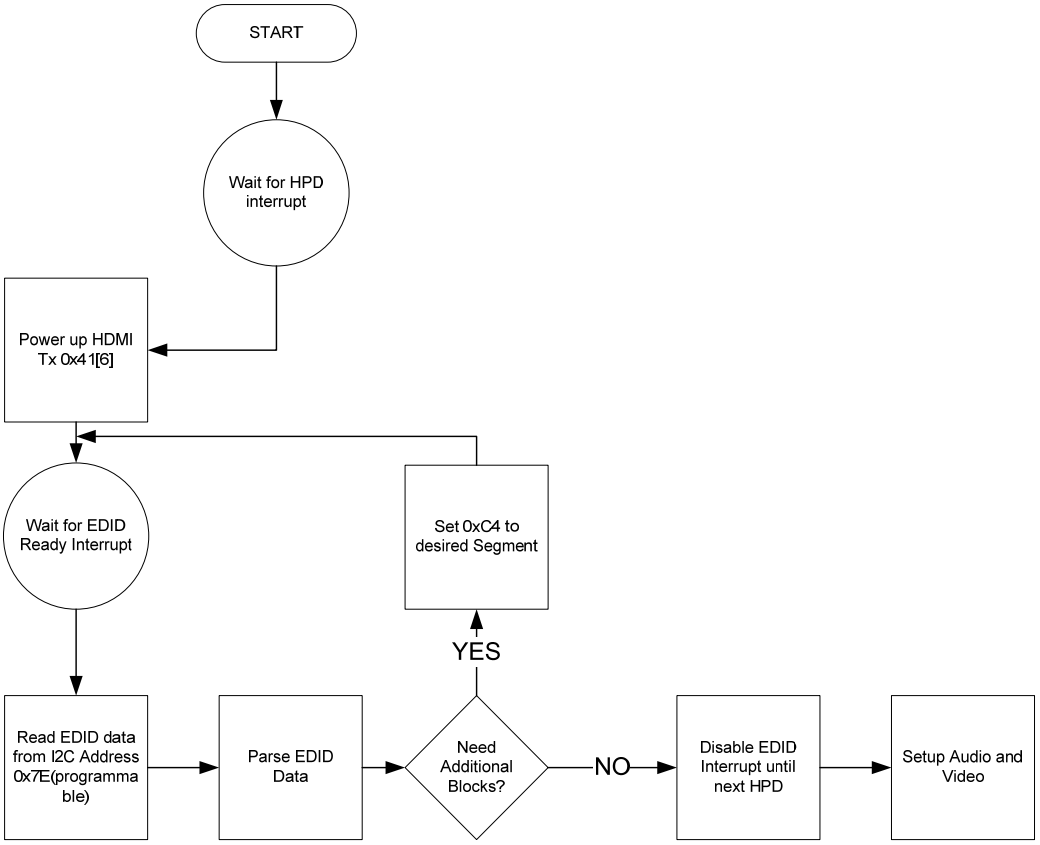
4.6.1.2 Additional Segments

EDID block 0 byte number 0x7E tells how many additional EDID blocks are available. If byte 0x7E is greater than 1, additional EDID segments will need to be read. If there is more than one segment, the second block (block 1) is required to be an EDID extension map. This map should be parsed according to the ▹ *VESA EDID* specifications to determine where additional EDID blocks are stored in the receiver's EDID EEPROM.

The ADV7511 is capable of accessing any of the up to 256 segments allowed by the ▹ EDID specification. By writing the desired segment number to register 0xC4, the ADV7511 will automatically access the correct portion of the EDID EEPROM over the DDC lines and load the 256 bytes into the EDID memory. When the action is complete, an EDID ready interrupt will occur to tell the user. If the host controller needs access to previously requested EDID information, then it can be stored in its own memory.

► Figure 25 shows how to implement software to read EDID from the receiver using the ADV7511.

Figure 25 Reading EDID through the ADV7511



4.6.1.3 EDID Tries Register (0xC9 [3:0])

The EDID Tries register limits the number of times the HDCP/EDID controller will try to read the EDID. Each time an EDID read fails with an I2C "Not Acknowledged" (NACK), this value is decremented. The default start-up value of this register is 3. Once the EDID Tries register is 0, the controller will not attempt to read the EDID until this register is set to something other than 0. This could be used if a sink asserts HPD before the DDC bus is ready resulting in several NACKs as the Tx attempts to read the EDID.

4.6.1.4 EDID Reread Register (0xC9[4])

If the EDID data is read in and the host determines that the data needs to be reread, this bit can be set from 0 to 1 for 10 times consecutively, and the current segment will be reread each time. This register should be toggled from 0 to 1 for 10 times consecutively to ensure a successful capture of the register value. This could be useful if the EDID checksum is calculated and determined not to match.

Another method to reread the EDID is to toggle the Main Power Down register bit (0x41[6]) from 0 to 1.

Table 93 EDID Handling Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x94	R/W	[2]	*****0**	EDID Ready Interrupt Enable	EDID Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x96	R/W	[2]	*****0**	EDID Ready Interrupt	EDID Ready Interrupt 0 = no interrupt detected 1 = interrupt detected
0xC4	R/W	[7:0]	00000000	EDID Segment	Sets the E-DDC segment used by the EDID Fetch routine.
0xC9	R/W	[4]	***0****	EDID Reread	Rereads current segment if toggled from 0 to 1 0 = disable 1 = enable
		[3:0]	****0011	EDID Tries	Maximum number of times that the EDID read will be attempted if unsuccessful.

4.7 HDCP Handling

4.7.1 For One Sink and No Upstream Devices

The ADV7511 has a built-in micro-controller to handle HDCP transmitter states, including handling down-stream HDCP repeaters. To activate HDCP from a system level the main controller needs to set the HDCP Desired register (0xAF[7]) to 1 and the Frame Encryption register (0xAF[4]) to 1, This informs the ADV7511 that the video stream should be encrypted. The ADV7511 takes control from there, and implements all of the remaining tasks defined by the HDCP 1.3 specification. Before sending audio and video, the BKSVs stored in registers 0xBF – 0xC3 should be compared with the revocation list which is compiled by managing System Renewability Messages (SRMs) provided on the source content (typically a DVD), and the BKSV Ready Interrupt register should be cleared. After the link is established, the system controller should monitor the status of HDCP by reading the HDCP Encrypted register (0xB8[6]) every two seconds. The DDC Controller Error Interrupt register (0x97[7]) will become active if there is an error relating to the controller. The meaning of the error can be determined by checking the DDC Controller Error register (0xC8[7:4]).

4.7.2 For Multiple Sinks and No Upstream Devices

When connecting the ADV7511 to a repeater, it is necessary to read all BKSV from downstream devices. These BKSVs must be checked against a revocation list, which will be provided on the source content.

The BKSV Count register (0xC7[6:0]) will read 0 when the first BKSV interrupt occurs. After the first BKSV interrupt is cleared, if the device is a repeater, a second BKSV interrupt will occur. The ADV7511 will automatically read up to 13 5-byte BKSVs at a time and store these in the EDID memory location (default location I2C address 0x7E). Refer to ► Table 94 for details about the location of the downstream BKSVs. The number of additional BKSVs currently stored in the EDID memory location can be read in register 0xC7[6:0]. If there are more than 13 additional BKSVs to be processed, the ADV7511 will collect the next up to 13 BKSVs across the DDC lines, then generate another interrupt when the next set is ready. There can be a maximum of 127 BKSVs total.

The BKVS Flag Interrupt register (0x97[6]) should be cleared by writing a 1 after each set of BKSVs is read. To check when authentication is complete, the system should monitor the register DDC Controller State register (0xC8[3:0]) and wait until this reaches state 4. At this time, the last step is to compare the BKSV list with the revocation list and then send the content.

Table 94 HDCP Related Register (EDID Memory Map)

Address	Type	Bits	Default Value	Register Name	Function
0x00	RO	[7:0]	0000000	BKSV0 – Byte 0	Downstream BKSV
0x01	RO	[7:0]	0000000	BKSV0 – Byte 1	…
0x02	RO	[7:0]	0000000	BKSV0 – Byte 2	…
0x03	RO	[7:0]	0000000	BKSV0 – Byte 3	…
0x04	RO	[7:0]	0000000	BKSV0 – Byte 4	…
0x05	RO	[7:0]	0000000	BKSV1 – Byte 0	…
…	…	…	…	…	…
0x60	RO	[7:0]	0000000	BKSV12 – Byte 0	…
0x61	RO	[7:0]	0000000	BKSV12 – Byte 1	…
0x62	RO	[7:0]	0000000	BKSV12 – Byte 2	…
0x63	RO	[7:0]	0000000	BKSV12 – Byte 3	…
0x64	RO	[7:0]	0000000	BKSV12 – Byte 4	…
0xF9	RO	[7]	0*******	BSTATUS Bit 7	Maximum Downstream Devices Exceeded (MAX_DEVS_EXCEEDED) 0 = Less than or equal to 127 devices 1 = More than 127 devices
		[6:0]	*0000000	BSTATUS Bits 6:0	Device Count (DEVICE_COUNT) Number of Downstream Devices
0xFA	RO	[7:5]	000*****	BSTATUS Bits 15:13	Reserved in HDCP 1.3 Specification
		[4]	***0****	BSTATUS Bit 12	HDMI Mode (HDMI_MODE) 0 = Sink is in DVI mode 1 = Sink is in HDMI mode
		[3]	****0***	BSTATUS Bit 11	Maximum Levels Exceeded (MAX_CASCADE_EXCEEDED) 0 = Less than or equal to 7 levels 1 = More than 7 levels
		[2:0]	*****000	BSTATUS Bits 10:8	Depth (DEPTH) Number of downstream levels

4.7.3 For Use in a Repeater

The ADV7511 can be used in a repeater, which is a device that has one or more HDMI Rx upstream from the ADV7511. To use the ADV7511 as a repeater, there are some additional requirements. The system software needs to pass the BKSVs of all downstream devices upstream through the repeater's receiver. In addition, the depth of the device tree and the total number of devices need to be communicated upstream. This depth and device count information can be found in the BSTATUS information, which is supplied in the EDID memory (default location I2C address 0x7E) at an offset of 0xF9 for the LSB's and 0xFA for the MSB's. ► Table 94 shows the meaning of the bits in the BSTATUS bit field.

The BSTATUS information is only available when the BKSVs are in the memory space. This is from the time there is a BKSV ready interrupt with BKSV Count register (0xC7[6:0]) greater than 0 to the time the interrupt flag is cleared. The EDID will not automatically be re-buffered. If the user would like to re-buffer an EDID segment the EDID re-read register described in section 4.6.1.4 should be used.

4.7.4 Software Implementation

► Figure 26 is a block diagram of HDCP software implementation for all cases using the ADV7511DDC Controller state machine. The necessary interactions with the ADV7511 registers and EDID memory as well as when these interactions should take place are covered in the block diagram. Note that there is no need to interact with the DDC bus directly, because all of the DDC functionality is controlled by the DDC Controller and follows the ▹ *HDCP specification 1.3*.

4.7.5 AV Mute

AV Mute can be enabled once HDCP authentication is completed. This can be used to maintain HDCP synchronization while changing video resolutions. While the BKSVs for downstream devices are being collected, an active HDCP link capable of sending encrypted video is established, but video should not be sent across the link until the BKSVs have been compared with the revocation list. It is not recommended to rely on AV mute to avoid sending audio and video during HDCP authentication. This is because AV Mute does not actually mute audio or video in the Tx. It requests the function from the Sink device. The best way to avoid sending unauthorized audio and video is to not send data to the ADV7511 inputs until authentication is complete. Another option is to use the color space converter to black out the video and disable the audio inputs to mute the audio. See ► 4.3.8.2 for how to black out the video, and see ► 4.3.10 for how to disable the various audio inputs.

4.7.6 HDCP Delay Control

During the HDCP authentication there are several steps. The default timing for these steps is sufficient to meet all HDCP requirements. However, in the case of unforeseen interoperability problems, control of the timing of several events is available. The Ri Checking Frequency can be controlled by setting 0xFC[7:6]. The range of available setting is in powers of 2 between once every 128 frames as default (0b00), to once every 16 frames (0b11). Ri Checking occurs soon after the leading edge of Vsync by default. Extra delay in units of Hsyncs can be added by setting the Ri Checking Position Delay register bits 0xFC[5:3]. After bit 0xAF[7] is set to 1 or an DDC Controller error interrupt occurs, usually the BKSV will be read immediately. Delay can be added before this read by setting register 0xFE[7:5]. After the BKSVS are read, the BCAPS is read immediately by default. Delay can be added here by setting register 0xFC[2:0]. After BCAPS is read the An value is written immediately by default. Delay can be added here by setting register 0xFD[7:5]. After the An write is completed, the AKSV is written immediately by default. Delay can be added here by setting 0xFD[4:2]. The time after AKSV is written before R_0 is read and the repeater timeout can be adjusted by register 0xD6[2:1].

Figure 26 HDCP Software Implementation

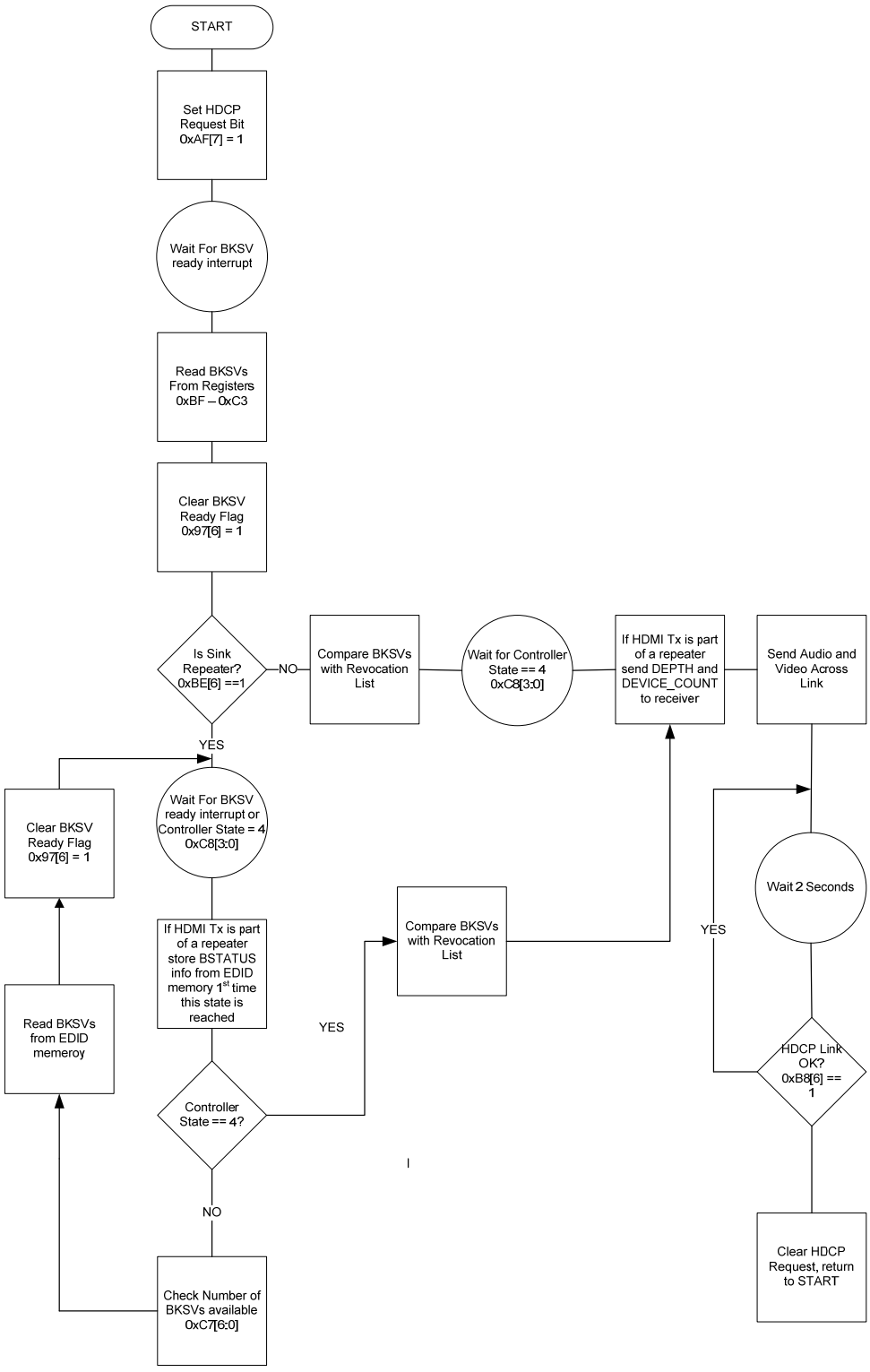


Table 95 HDCP Handling Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x94	R/W	[1]	******0*	HDCP Authenticated Interrupt Enable	HDCP Authenticated Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x95	R/W	[6]	*0******	BKSV Flag Interrupt Enable	BKSV Flag Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x96	R/W	[1]	******0*	HDCP Authenticated	HDCP Authenticated 0 = no interrupt detected 1 = interrupt detected
0x97	R/W	[6]	*0******	BKSV Flag Interrupt	BKSV Flag Interrupt 0 = no interrupt detected 1 = interrupt detected
0xAF	R/W	[7]	0*******	HDCP Enable	Enable HDCP 0 = HDCP Disabled 1 = HDCP Encryption Enabled
		[4]	***1****	Frame Encryption	Enable HDCP Frame Encryption 0 = Current Frame NOT HDCP Encrypted 1 = Current Frame HDCP Encrypted
0xB0	RO	[7:0]	00000000	Byte 0 of An or AKSV Byte 0	Byte 0 of An or AKSV Byte 0
0xB1	RO	[7:0]	00000000	Byte 1 of An or AKSV Byte 1	Byte 1 of An or AKSV Byte 1
0xB2	RO	[7:0]	00000000	Byte 2 of An or AKSV Byte 2	Byte 2 of An or AKSV Byte 2
0xB3	RO	[7:0]	00000000	Byte 3 of An or AKSV Byte 3	Byte 3 of An or AKSV Byte 3
0xB4	RO	[7:0]	00000000	Byte 4 of An or AKSV Byte 4	Byte 4 of An or AKSV Byte 4
0xB5	RO	[7:0]	00000000	Byte 5 of An	byte 5 of An
0xB6	RO	[7:0]	00000000	Byte 6 of An	byte 6 of An
0xB7	RO	[7:0]	00000000	Byte 7 of An	byte 7 of An
0xB8	RO	[6]	*0******	HDCP Encryption Status	1 means the A/V content is being encrypted at present. 0 = A/V Not Encrypted 1 = A/V Encrypted
		[4]	***0****	Key Read Error	1 means HDCP key reading error. 0 = Read HDCP Keys Correctly 1 = Errors Encountered Reading HDCP Keys
0xBA	R/W	[2]	*****0**	Display AKSV	Show AKSV in registers 0xB0 to 0xB4, Check Ri' before and after update, Must be set to Default 0 = Don't Show AKSV 1 = Show AKSV in 0xB0 - 0xB4
		[1]	******0*	Ri Two Point Check	Ri Two Point Check. Check Ri' before and after update. 0 = HDCP Ri standard

Address	Type	Bits	Default Value	Register Name	Function
					1 = enable HDCP Ri two point check
0xBE	RO	[7:0]	00000000	BCAPS	HDCP related register [7] Reserved, [6] Repeater, [5] BKSV FIFO ready, [4] Fast DDC Bus, [3:2] Reserved, [1] HDCP 1.1 Features, [0] Fast Re-Authentication.
0xBF	RO	[7:0]	00000000	BKSV Byte 0	Bksv read from Rx by the DDC Controller
0xC0	RO	[7:0]	00000000	BKSV Byte 1	Bksv read from Rx by the DDC Controller
0xC1	RO	[7:0]	00000000	BKSV Byte 2	Bksv read from Rx by the DDC Controller
0xC2	RO	[7:0]	00000000	BKSV Byte 3	Bksv read from Rx by the DDC Controller
0xC3	RO	[7:0]	00000000	BKSV Byte 4	Bksv read from Rx by the DDC Controller
0xC7	RO	[6:0]	*0000000	BKSV Count	BKSVs Available in Sink's BKSV FIFO
0xC8	RO	[7:4]	0000****	DDC Controller Error	DDC Controller Error Error code report when the DDC Controller Error Interrupt register 0x97[7] = 1
		[3:0]	****0000	DDC Controller State	DDC Controller State State of the controller used for HDCP debug purposes
0xCA	RO	[7:0]	00000000	HDCP BSTATUS[15:8]	BSTATUS information for HDCP [15:8]
0xCB	RO	[7:0]	00000000	HDCP BSTATUS[7:0]	BSTATUS information for HDCP [7:0]
0xFC	R/W	[7:6]	00******	Ri Checking Frequency	Ri Checking Frequency 00 = 128 frames 01 = 64 frames 10 = 32 frames 11 = 16 frames
		[5:3]	**000***	Ri Checking Position Delay	Ri Checking Position Delay in Units of Hsync 0 = no delay 1 = 8 Hsyncs 2 = 16 Hsyncs 3 = 32 Hsyncs 4 = 64 Hsyncs 5 = 128 Hsyncs 6 = 256 Hsyncs 7 = 512 Hsycns
		[2:0]	*****000	BCAPS Read Delay	Delay Between Reading of BKSV and BCAPs 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
0xFD	R/W	[7:5]	000*****	An Write Delay	Delay Between Reading of BCAPS and Writing of An 000 = no delay

Address	Type	Bits	Default Value	Register Name	Function
					001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
		[4:2]	***000**	AKSV Write Delay	Delay Between Writing of An and Writing of AKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
0xFE	R/W	[7:5]	000*****	HDCP Start Delay	Delay Between Setting Enable HDCP Register 0xAF[7] = 1 and Reading of BKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms

4.8 Power Management

The ADV7511 has a Main Power Down, as well as additional methods, which can be used to further achieve power savings. The Main Power-Down section describes the method and results of using Main Power Down. The Additional Power-Down Methods section describes the methods and trade-offs for achieving minimum power consumption.

4.8.1 Main Power-Down

The ADV7511 can put into the Main Power-Down mode by the power-down pin or by register 0x41[6]. The ADV7511 will power down if either the pin or register are active, but will only power up if both are inactive. Also the ADV7511 can only be powered up if the HPD pin is 1. The conditions for Main Power Down are shown in Table 96.

The ADV7511 power-down pin polarity depends on the chip I2C address selection. If the user wants to use 0x72, then the PD/AD pin is active high. If the user wants to use 0x7A, the PD/AD pin is active low. The power-down pin polarity can be verified by reading register 0x42[7]. See the *ADV7511 Hardware User's Guide* for more information about the PD/AD pin and power specifications.

Some registers will be reset when the device is put into the Main Power-Down mode. Which registers are reset and which registers retain their values depends on the method of power down used. The details are in ► Table 97.

Table 96 Main Power Down Conditions

HPD Pin	Power Down Register (0x41[6], 1 = Power Down)	Power Down Pin (1 = Power Down)	Result
0	0	0	Main Power Down
0	0	1	Main Power Down
0	1	0	Main Power Down
0	1	1	Main Power Down
1	0	0	Main Power Up
1	0	1	Main Power Down
1	1	0	Main Power Down
1	1	1	Main Power Down

Table 97 Register Reset Control

Address	HPD Pin = 0 or Power Down Pin Active	Power Down Register 0x41[1]	CEC Power Down Register 0xE2[0]
Main Register Map			
0x00 – 0x93	Reset	Not Reset	Not Reset
0x94 - 0x97 (except 0x96[7:6] and 0x97[5:0])	Reset	Reset	Not Reset
0x96[7:6] and 0x97[5:0]	Not Reset	Not Reset	Not Reset
0x98 – 0xAE	Not Reset	Not Reset	Not Reset
0xAF-0xCC	Reset	Reset	Not Reset
0xCD -0xF8	Not Reset	Not Reset	Not Reset
0xF9 – 0xFE	Reset	Not Reset	Not Reset
Packet Memory Map			
0x00 – 0xFF	Reset	Reset	Not Reset
CEC Memory Map			
0x00 – 0xFF	Not Reset	Not Reset	Reset

4.8.2 Additional Power Down Methods

An ultra-low power down level can be achieved by setting the Monitor Sense Power Down register (0xA1[6]) to 1. As a tradeoff interrupt handling and Monitor Sense monitoring cannot be used. With Monitor Sense Power-Down active, the HPD State register (0x42[6]) is still valid. Polling of this register can be used to determine if a Sink is connected.

If SPDIF is not being used, the SPDIF Enable register (0x0B[7]) can be set to 0. This will turn off the SPDIF receiver. This is not necessary during main power-down mode as the SPIDF receiver will be already powered down. CEC can be powered on and off independent from the Main Power Down mode. If CEC is not being used, then the CEC Power Down bit (0xE2[0]), can be set to 1.

If the inputs to the ADV7511 are toggling while the HDMI Tx is in power down mode, some power will be consumed. If there is no way to disable the toggling of the data and clock input video, then clock gating can be used to reduce power. This is activated by setting the Video Input and Clock Gating register (0xD6[0]) to 1. Similarly the CEC clock toggling will consume some power. Disabling or reducing the speed of this clock will further save power during power down mode.

Table 98 Additional Power Down Methods and Effects

Power Reductions Method	Power Reduction Trade Off
Monitor Sense Power Down (0xA1[6]) = 1	-Interrupts Cannot be used -Registers 0x94 – 0x97 invalued -Monitor Sense State (0x42[5]) is invalid
SPDIF Enable (0x0B[7]) = 0	-SPDIF Cannot be used
Input Clock Gating (0xD6[0])	-Video Cannot be Used
CEC Power Down (0xE2[0])	CEC Cannot be used
Disable CEC Clock	CEC Cannot be used

Table 99 Power Management Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x41	R/W	[6]	*1******	POWER DOWN	Main Power Down 0 = all circuits powered up 1 = power down whole chip, except I2C,HPD interrupt,Monitor Sense interrupt,CEC 0 = Normal Operation 1 = ADV7511 Powered Down
0x42	RO	[7]	1*******	Power Down Polarity	Polarity for chip pin , Default is 1 0 = active low 1 = active high
0xA1	R/W	[6]	*0******	Monitor Sense Power Down	Monitor Sense Power Down 0 = Monitor Sense monitoring enabled 1 = Monitor Sense monitoring disabled
0xD6	R/W	[0]	*******0	Audio and Video Input Gating	Audio and Video Input Gating 0 = video input and clock not gated 1 = video input and clock gated

4.9 CEC Processing

Consumer Electronic Control (CEC) is a single-wire, bidirectional interface intended to facilitate the control of any device on an HDMI network, as shownin ►Figure 27, with the remote control unit or on-device control buttons of any other device connected to the network. Defined as an optional feature in the HDMI specification, it is based on the AV Link function defined in the European SCART (Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs) specification. ►Table 100describes some typical end-user CEC features.

Figure 27 Typical All-HDMI Home Theatre

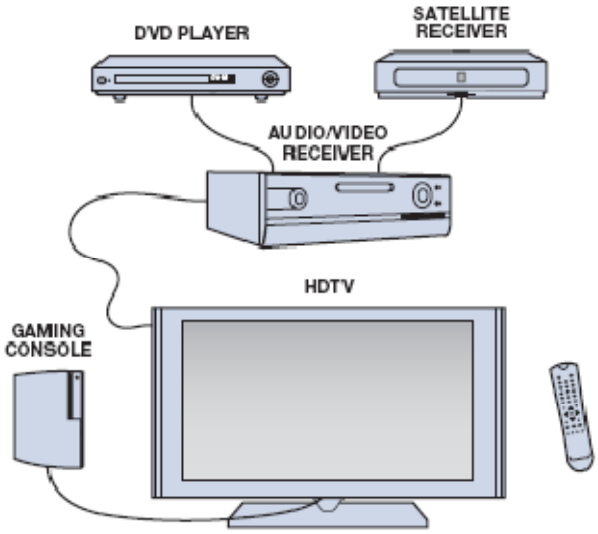


Table 100 Some typical"End-User" CEC Features:

Feature	*Description*
One-Touch Play	*Pushing the "play" button commands a source to play and become the active video source for the TV.*
Stand-By	*Pushing the "power down" button of any active device commands all devices on the HDMI network to shut down.*
One-Touch Record	*Pushing the "record" button commands a recording device to power up and record the content currently displayed on the TV.*

Many of these end-user features require sending multiple messages over the CEC bus such as "Active Source," and "Routing Change," which support the CEC feature "Routing Control." This feature allows a device to play and become the active source by switching the TV's source input. If the TV is displaying another source at the time this command is used, it may place the other source into "stand-by" mode, depending on the implementation. Please see the CEC section of the HDMI 1.4 specification for details about CEC itself.

4.9.1 CEC Addressing

On receiving the HPD Interrupt, the system software has to parse the EDID from the sink to determine the CEC device's Physical Address. Once this is done, the Logical Address is determined using a polling method as defined in the HDMI Specification. Once the Logical Address is determined, it is programmed in to the Logical Address (0x4C[7:4]) register. The ADV7511 allows the system to configure three separate Logical Addresses which can then be selected using the Logical Address Mask (0x4B[6:4]) register. This allows the system to emulate up to three separate CEC devices using the same CEC module.

4.9.2 CEC Transmitter

The CEC Transmitter module is used to describe the CEC messages when the on-chip CEC device acts as an initiator. The host utilizes this module to transmit directly addressed messages or broadcast messages on the CEC bus.

4.9.2.1 CEC Transmitter Setup and Control

If the host wants to send a message to other CEC devices, the host should write the message to the CEC Tx Frame Data[0:14] registers (0x01 -0x0F) and other CEC Tx-related control registers one by one. Finally, it will enable the transmission process through setting the register bit of CECTx Transmission Enable (0x11[0]) to '1'. Then the CEC Tx module will kick off the transmission process.

4.9.2.2 CEC Transmitter Interrupt Handling

When the message transmission is completed or any error occurs, the CEC Tx module will flag an interrupt signal to the host. There are three kinds of interrupt sources in this module. These are Tx Ready, Tx Arbitration Lost, and Tx Retry Timeout. The Tx Ready interrupt means that the message in the Tx buffer has been transmitted successfully and the CEC Tx module has been ready to accept and transmit the next message. The Tx Arbitration Lost interrupt means that arbitration has been lost to another initiator, when one or more other initiators are trying to access the bus at the same time as the ADV7511. The CEC Tx module will stop transmitting and become a follower. The Tx Retry Timeout interrupt means that the initiator has tried to transmit the message and retried up to the number of times, which is indicated by the Tx Retry register, with no acknowledge. The reason for the failure is either due to a "no acknowledge" flagged by the follower, or low drive occurring on CEC bus. The Tx Nack Counter shows how many times the transmission has failed because of a "no acknowledge." The Tx Lowdrive Counter shows how many times the transmission has failed because of low drive.

For these three interrupt types, only one can occur at a time, and the CEC Tx module will stop the transmission process immediately. According to the interrupt type, the host must decide how to process the interrupt. ► Figure 28is the state machine for control of the CEC message transmission process.

Figure 28 CEC Transmitter State Machine

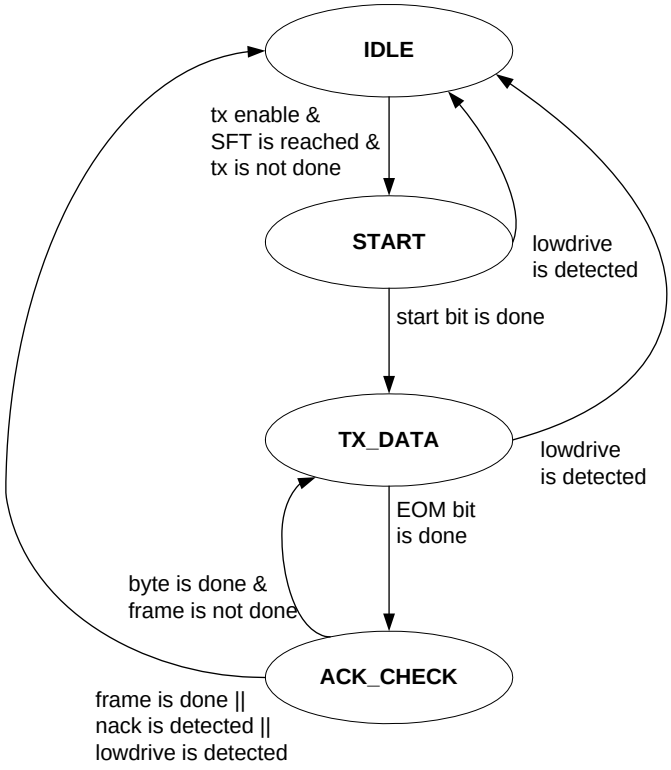


Table 101 CEC Transmitter Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function

0x95	R/W	[5]	**0*****	Tx Ready Interrupt Enable	CEC Tx Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[4]	***0****	Tx Arbitration Lost Interrupt Enable	CEC Tx Arbitration Lost Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[3]	****0***	Tx Retry Timeout Interrupt Enable	CEC Tx Retry Timeout Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x97	R/W	[5]	**0*****	Tx Ready Interrupt	CEC Tx Ready Interrupt 0 = no interrupt detected 1 = interrupt detected
		[4]	***0****	Tx Arbitration Lost Interrupt	CEC Tx Arbitration Lost interrupt 0 = no interrupt detected 1 = interrupt detected
		[3]	****0***	Tx Retry Timeout Interrupt	CEC Tx Retry Timeout interrupt 0 = no interrupt detected 1 = interrupt detected

Table 102 CEC Transmitter Related Registers (CEC Map)

Address	Type	Bits	Default Value	Register Name	Function
0x00	R/W	[7:0]	00000000	CEC Tx Frame Header	CEC Tx Header
0x01	R/W	[7:0]	00000000	CEC Tx Frame Data 0	CEC Tx Opcode
0x02	R/W	[7:0]	00000000	CEC Tx Frame Data 1	CEC Message Operand 1
0x03	R/W	[7:0]	00000000	CEC Tx Frame Data 2	CEC Message Operand 2
0x04	R/W	[7:0]	00000000	CEC Tx Frame Data 3	CEC Message Operand 3
0x05	R/W	[7:0]	00000000	CEC Tx Frame Data 4	CEC Message Operand 4
0x06	R/W	[7:0]	00000000	CEC Tx Frame Data 5	CEC Message Operand 5
0x07	R/W	[7:0]	00000000	CEC Tx Frame Data 6	CEC Message Operand 6
0x08	R/W	[7:0]	00000000	CEC Tx Frame Data 7	CEC Message Operand 7
0x09	R/W	[7:0]	00000000	CEC Tx Frame Data 8	CEC Message Operand 8
0x0A	R/W	[7:0]	00000000	CEC Tx Frame Data 9	CEC Message Operand 9
0x0B	R/W	[7:0]	00000000	CEC Tx Frame Data 10	CEC Message Operand 10
0x0C	R/W	[7:0]	00000000	CEC Tx Frame Data 11	CEC Message Operand 11
0x0D	R/W	[7:0]	00000000	CEC Tx Frame Data 12	CEC Message Operand 12
0x0E	R/W	[7:0]	00000000	CEC Tx Frame Data 13	CEC Message Operand 13
0x0F	R/W	[7:0]	00000000	CEC Tx Frame Data 14	CEC Message Operand 14
0x10	R/W	[4:0]	***00000	CEC Tx Frame Length	CEC Tx Message Size
0x11	R/W	[0]	*******0	CEC Tx Transmission Enable	CEC Tx Enable 0 = Do not transmit CEC frame in Tx buffer 1 = Transmit CEC frame in Tx buffer
0x12	R/W	[6:4]	*001****	CEC Tx Retry	CEC Tx Retry
		[3:0]	****0011	CEC Tx Retry Signal Free Time	Signal Free Time Period for retransmission retry
0x13	R/W	[7:4]	0101****	CEC Tx SFT5	Signal Free Time of 5 periods SFT5: New initiator wants to send a frame
		[3:0]	****0111	CEC Tx SFT7	Signal Free Time of 7 periods SFT7: Present Initiator wants to send another frame immediately after its previous frame.
0x14	RO	[7:4]	0000****	CEC Tx Lowdrive Counter	Report error times in case of low impedance detection This is automatically cleared upon sending next message.
		[3:0]	****0000	CEC Tx NACK Counter	Report Error Times In Case of Negative Acknowledge

4.9.3 CEC Receiver

The CEC Rx module is used to retrieve CEC messages from the CEC bus when the on-chip CEC device acts as a follower. The host utilizes this module to receive both broadcast messages and messages directly addressed to the ADV7511. The on-chip CEC Rx module is equipped with three internal 16-byte frame buffers which can be used to improve system latency for CEC message processing and reduce the likelihood of dropping messages.

4.9.3.1 CEC Receiver Setup and Control

The CEC Receiver module is enabled by setting 0x4E[1:0] = 0b01 if the CEC clock is enabled and timing parameters match the clock frequency. The CEC Rx module will then monitor the CEC bus and accept the broadcast messages or messages addressed directly to the device with the HDMI Tx.

To enable usage of all three internal frame buffers, the Use all CEC Rx Buffers (0x4A[3]) bit must be set. To provide information on the order of arrival of a new frame in each buffer, three two-bit timestamp registers are available (0x26[5:0]). Each timestamp register can contain a value between and including 0b01 and 0b11, depending on when a new frame arrives at the corresponding CEC Rx Buffer. The earliest frame arrival is assigned a value of 0b01, and the latest frame arrival is assigned a value of 0b11. A value of 0b00 for the timestamp indicates that no frame is currently present in the respective CEC Rx Buffer. See Section ► 4.9.3.2.for more details on timestamp operation and processing.

Registers 0x77 – 0x7E are used to set pre-defined Wake Up Opcodes for the CEC Rx module. When an opcode which is defined in these registers is received, a corresponding interrupt (0x93[7:0] in the Main Register Map) is generated. This feature is not required for full featured CEC operation.

4.9.3.2 CEC Receiver Message Processing and Interrupt Handling

When any message besides a polling message is completely buffered in one of the CEC Rx Buffers, the CEC Receiver module will set the corresponding CEC Rx Buffer Ready bit (0x49[2:0]), and also assert the corresponding CEC Rx Buffer Ready Interrupt bit (0x97[2:0] Main Register Map).

Received CEC messages can be accessed from the CEC Rx Frame Buffer registers:

Buffer 1 – CEC Rx Buffer Frame Header + Data (0x15 – 0x24)

Buffer 2 – CEC Rx Buffer Frame Header + Data (0x27- 0x36)

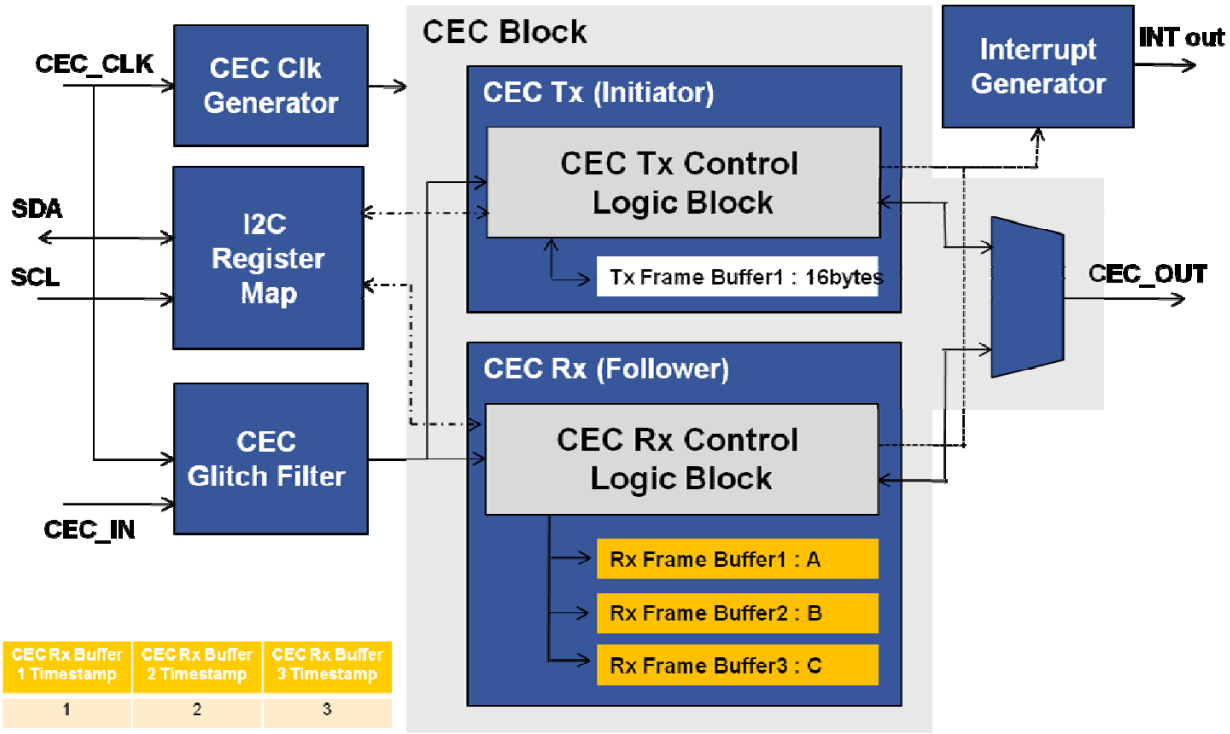
Buffer 3 – CEC Rx Buffer Frame Header + Data (0x38 – 0x47)

Once the host processes the recently arrived frame (or earlier frame arrivals), the host system must clear the CEC Rx Buffer Ready bit (0x49[2:0]) by toggling the value of the corresponding CEC Rx Buffer Ready Clear (0x4A[2:0]) bit. Toggling the CEC Rx Buffer Ready Clear bit (0x4A[2:0]) resets the value of the respective timestamp to '0'. For example, when the CEC Rx Buffer 3 Ready Clear (0x4A[2]) bit is toggled, the CEC Rx Buffer 3 Timestamp (0x26[5:4]) gets reset to 0b00, and the CEC Rx Buffer 3 Ready bit (0x49[2]) also gets reset to 0b0. Timestamp values are only updated when a new frame arrives.

Once the host processes the recently arrived frame (or earlier frame arrivals), the host system must also clear the corresponding CEC Rx Buffer Ready Interrupt bit (0x27[2:0] Main Map). See ►Section 4.10 for details on using interrupts. Clearing the CEC Rx Buffer Ready Interrupt bit (0x27[2:0] Main Map) causes the INT pin to go low thereby allowing the host system to process other interrupts.

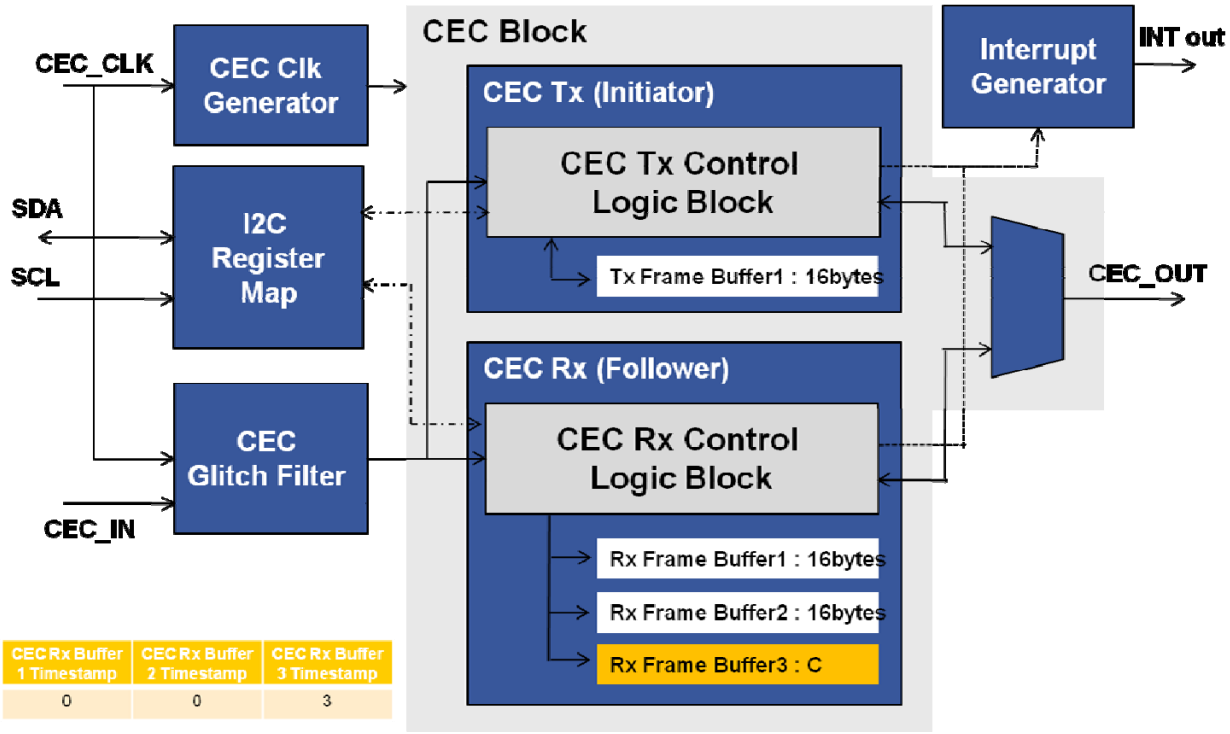
► Figure 29 to ►Figure 31 illustrate the behavior of the CEC Rx Buffer Timestamp (0x26[5:0]) registers.

Figure 29 **CEC Receiver Timestamp Operation – Message Arrival**



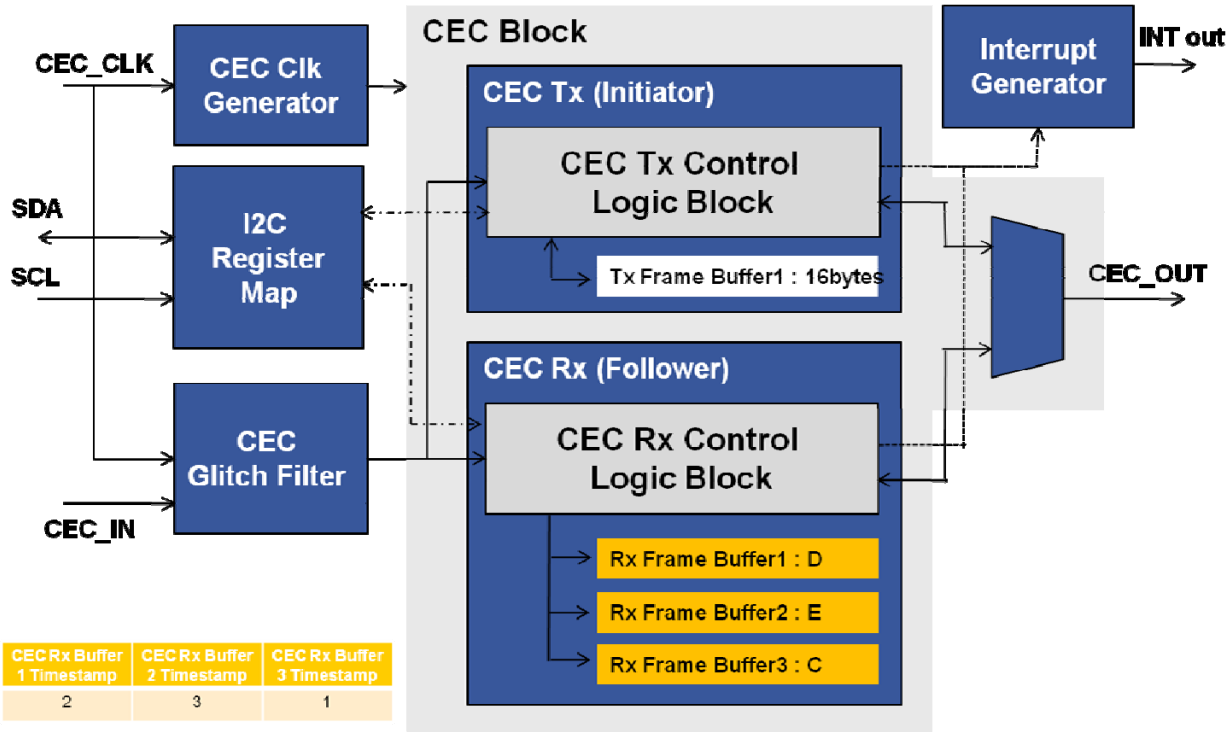
As shown ►Figure 29, once messages arrive and fill up the three CEC Rx Buffers, timestamp values are assigned to the corresponding CEC Rx Buffer Timestamp (0x26[5:0]) registers with the earliest arrival being assigned a value of 1, and later arrivals being assigned incrementally higher integer values. In the example shown in ►Figure 29, message "A" is the earliest arrival at CEC Rx Buffer 1 and therefore CEC Rx Buffer 1 Timestamp (0x26[1:0]) assumes a value of '1'. Messages "B" and "C" are subsequent arrivals and their corresponding timestamp registers assume values of '2' and '3' respectively.

Figure 30 CEC Receiver Timestamp Operation – Partial Message Processing



► Figure 30shows the status of the CEC Rx Buffer Timestamp registers once the corresponding messages have been processed by the system host and the corresponding CEC Rx Buffer Ready Clear (0x4A[2:0]) bits have been toggled. As can be seen in ► Figure 30, toggling the CEC Rx Buffer Ready Clear bit resets the respective timestamp value to '0' and readies the CEC Rx Buffer to receive a new message. Note that the corresponding CEC Rx Buffer Ready Interrupt (0x97[2:0] – Main Map) also has to be cleared to cause the INT pin to go low and allow the system host to continue processing other system interrupts.

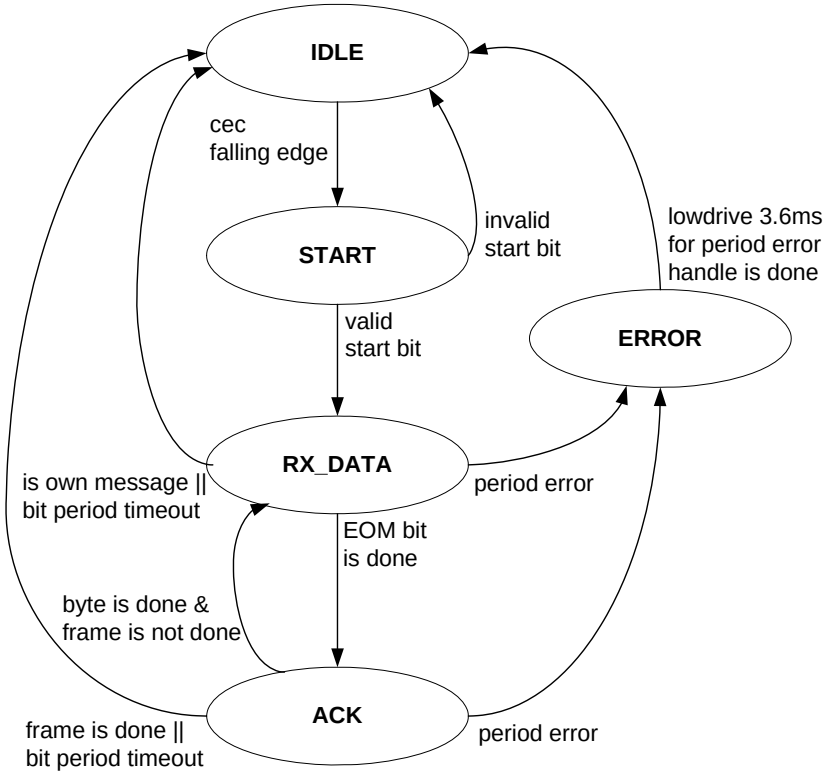
Figure 31 **CEC Receiver Timestamp Operation – New Message Arrival**



►Figure 31 shows the status of the CEC Rx Buffer Timestamps once new messages have arrived into the CEC Rx Buffers. As seen in ►Figure 31, the value of CEC Rx Buffer 3 timestamp is assigned a value of '1', since it is the earliest available message. The timestamp values corresponding to the new message arrivals at CEC Rx Buffers 1 and 2 are assigned values of '2' and '3' respectively.

► Figure 32 illustrates the state machine for control of the CEC message receiving process.

Figure 32 CEC Receiver State Machine



4.9.3.3 Handling CEC Initiators with non-compliant EOM

The CEC hardware does not check for an End of Message (EOM) signal to identify the end of a message. Instead the CEC Rx will continue to buffer bytes until a "time out" occurs. This could cause a problem for the HDMI compliance test because bytes sent after an EOM should be ignored.

The following procedure can be used to work around issues with non HDMI compliant CEC sources, which continue sending data after the EOM signal.

1. Read the message opcode in the corresponding Rx Frame Buffer register
2. Check expected length of message in HDMI 1.4 Specification Supplement 1
3. Compare expected length with length reported in the corresponding Rx Frame Buffer Frame Length register
4. If the expected length is greater than the reported length, then use the expected length

Table 103 CEC Receiver Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x95	R/W	[2]	*****0**	Rx Ready 3 Interrupt Enable	CEC Rx Ready 3 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[1]	******0*	Rx Ready 2 Interrupt Enable	CEC Rx Ready 2 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[0]	*******0	Rx Ready 1 Interrupt Enable	CEC Rx Ready 1 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x97	R/W	[2]	*****0**	Rx Ready 3 Interrupt	CEC Rx Ready 3 Interrupt 1 = interrupt detected for rx buffer 3 0 = no interrupt detected for buffer 3 1 = interrupt detected for buffer 3 0 = no interrupt detected for buffer 3
		[1]	******0*	Rx Ready 2 Interrupt	CEC Rx Ready 2 Interrupt 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2
		[0]	*******0	Rx Ready 1 Interrupt	CEC Rx Ready 1 Interrupt 1 = interrupt detected for rx buffer 1 0 = no interrupt detected for buffer 1 1 = interrupt detected for buffer 1 0 = no interrupt detected for buffer 1

Table 104 CEC Receiver Related Registers (CEC Map)

Address	Type	Bits	Default Value	Register Name	Function
0x15	RO	[7:0]	00000000	CEC Rx Buffer 1 Frame Header	Rx Header Block in the Frame (Buffer 1)
0x16	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 0	Rx Data Opcode (Buffer 1)
0x17	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 1	Received CEC Operand 1(Buffer 1)
0x18	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 2	Received CEC Operand 2 (Buffer 1)
0x19	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 3	Received CEC Operand 3 (Buffer 1)
0x1A	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 4	Received CEC Operand 4 (Buffer 1)
0x1B	RO	[7:0]	00000000	CEC Rx Frame Buffer 1	Received CEC Operand 5 (Buffer 1)

Address	Type	Bits	Default Value	Register Name	Function
				Data byte 5	
0x1C	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 6	Received CEC Operand 6 (Buffer 1)
0x1D	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 7	Received CEC Operand 7 (Buffer 1)
0x1E	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 8	Received CEC Operand 8 (Buffer 1)
0x1F	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 9	Received CEC Operand 9 (Buffer 1)
0x20	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 10	Received CEC Operand 10 (Buffer 1)
0x21	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 11	Received CEC Operand 11 (Buffer 1)
0x22	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 12	Received CEC Operand 12 (Buffer 1)
0x23	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 13	Received CEC Operand 13 (Buffer 1)
0x24	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 14	Received CEC Operand 14 (Buffer 1)
0x25	RO	[4:0]	***00000	CEC Rx Buffer 1 Frame Length	Rx Message Size (Buffer 1) Number of operands + 2
0x26	RO	[6]	*1******	CEC Rx Enable	RX enable 0 = The CEC module is currently not able to receive a new CEC frame 1 = The CEC module is currently able to receive a new CEC frame
		[5:4]	**00****	CEC Rx Buffer 3 Timestamp	Specifies the order in which the message in Buffer 3 was received relative to Buffer 1 and Buffer 2 for the current buffered messages 00 = No valid message 01 = Oldest received buffered message 10 = Second most Recent received buffered message 11 = Most Recent received buffered message
		[3:2]	****00**	CEC Rx Buffer 2 Timestamp	Specifies the order in which the message in Buffer 2 was received relative to Buffer 1 and Buffer 3 for the current buffered messages 00 = No valid message 01 = Oldest received buffered message 10 = Second most Recent received buffered message 11 = Most Recent received buffered message
		[1:0]	******00	CEC Rx Buffer 1 Timestamp	Specifies the order in which the message in Buffer 1 was received relative to Buffer 2 and Buffer 3 for the current buffered messages 00 = No valid message 01 = Oldest received buffered message 10 = Second most Recent received buffered message 11 = Most Recent received buffered message

Address	Type	Bits	Default Value	Register Name	Function
0x27	RO	[7:0]	00000000	CEC Rx Buffer 2 Frame Header	Rx Header Block in the Frame (Buffer 2)
0x28	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 0	Rx Data Opcode (Buffer 2)
0x29	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 1	ReceivedCEC Operand 1(Buffer 2)
0x2A	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 2	ReceivedCEC Operand 2 (Buffer 2)
0x2B	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 3	Received CEC Operand 3 (Buffer 2)
0x2C	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 4	Received CEC Operand 4 (Buffer 2)
0x2D	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 5	Received CEC Operand 5 (Buffer 2)
0x2E	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 6	Received CEC Operand 6 (Buffer 2)
0x2F	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 7	Received CEC Operand 7 (Buffer 2)
0x30	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 8	Received CEC Operand 8 (Buffer 2)
0x31	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 9	Received CEC Operand 9 (Buffer 2)
0x32	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 10	Received CEC Operand 10 (Buffer 2)
0x33	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 11	Received CEC Operand 11 (Buffer 2)
0x34	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 12	Received CEC Operand 12 (Buffer 2)
0x35	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 13	Received CEC Operand 13 (Buffer 2)
0x36	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 14	Received CEC Operand 14 (Buffer 2)
0x37	RO	[4:0]	***00000	CEC Rx Buffer 2 Frame Length	Rx Message Size (Buffer 2) Number of operands + 2
0x38	RO	[7:0]	00000000	CEC Rx Buffer 3 Frame Header	Rx Header Block in the Frame (Buffer 3)
0x39	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 0	Rx Data Opcode (Buffer 3)

Address	Type	Bits	Default Value	Register Name	Function
0x3A	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 1	Received CEC Operand 1(Buffer 3)
0x3B	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 2	Received CEC Operand 2 (Buffer 3)
0x3C	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 3	Received CEC Operand 3 (Buffer 3)
0x3D	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 4	Received CEC Operand 4 (Buffer 3)
0x3E	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 5	Received CEC Operand 5 (Buffer 3)
0x3F	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 6	Received CEC Operand 6 (Buffer 3)
0x40	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 7	Received CEC Operand 7 (Buffer 3)
0x41	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 8	Received CEC Operand 8 (Buffer 3)
0x42	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 9	Received CEC Operand 9 (Buffer 3)
0x43	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 10	Received CEC Operand 10 (Buffer 3)
0x44	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 11	Received CEC Operand 11 (Buffer 3)
0x45	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 12	Received CEC Operand 12 (Buffer 3)
0x46	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 13	Received CEC Operand 13 (Buffer 3)
0x47	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 14	Received CEC Operand 14 (Buffer 3)
0x48	RO	[4:0]	***00000	CEC Rx Buffer 3 Frame Length	Rx Message Size (Buffer 3) Number of operands + 2
0x49	RO	[2]	*****0**	CEC Rx Buffer 3 Ready	Indicates frame presence in Buffer 3 0 = No CEC frame available in buffer 3 1 = A CEC frame is available in buffer 3
		[1]	******0*	CEC Rx Buffer 2 Ready	Indicates frame presence in Buffer 2 0 = No CEC frame available in buffer 2 1 = A CEC frame is available in buffer 2
		[0]	*******0	CEC Rx Buffer 1 Ready	Indicates frame presence in Buffer 1 0 = No CEC frame available in buffer 1 1 = A CEC frame is available in buffer 1

Address	Type	Bits	Default Value	Register Name	Function
0x4A	R/W	[3]	****1***	Use all CEC Rx Buffers	Choose whether the new frames should be received in all 3 buffers or only one buffer 0 = Use only buffer 0 to store CEC frames (Legacy mode) 1 = Use all 3 buffers to stores the CEC frames (Non-legacy mode)
		[2]	*****0**	CEC Rx Buffer 3 Ready Clear	Set high to clear 0x49[2] and reset 0x26[5:4] 0 = Retain the value of 0x49[2] 1 = Clear out 0x49[2]
		[1]	******0*	CEC Rx Buffer 2 Ready Clear	Set high to clear 0x49[1] and reset 0x26[3:2] 0 = Retain the value of 0x49[1] 1 = Clear out 0x49[1]
		[0]	*******0	CEC Rx Buffer 1 Ready Clear	Set high to clear 0x49[0] and reset 0x26[1:0] 0 = Retain the value of 0x49[0] 1 = Clear out 0x49[0]

4.9.4 Typical Operation Flow

4.9.4.1 CEC Acting as an Initiator:

Step 1

The host writes the message to the Tx Frame Header (0x00 CEC Memory Map) and Tx FrameData[0:14] registers. Then the Tx Enable register (0x11[0] CECMemory Map) will be set to '1' to enable the CEC Tx module.

Step 2

When CEC module detects that the host has set the Tx Enable signal to be valid, it will begin to send the message in the Tx buffer after waiting for the signal free time. During the message transmission, if CEC bus arbitration is lost, CEC Tx module will stop the transmission operation immediately and interrupt the host through setting Tx Arbitration Lost signal. If no acknowledge signal is received or lowdrive is detected although TX has tried Tx Retry (0x12[6:4] CEC Memory Map) times, the CEC Tx module will report that the transmission is failed through setting the interrupt signal of Tx Retry Timeout. If the message transmission is successful, the Tx Ready interrupt signal will be set to notify the host.

Step 3

The host will be interrupted once the message has been completed whether it is successful of not. Then the host is responsible for deciding what to do next according to the interrupt type. The Tx Nack Counter and Tx Lowdrive Counter show complementary information to the host so that the host can know how many times the transmission has failed due to no acknowledge and how many times the transmission has failed due to low drive. These two counters play an important role during the operation of logical address allocation. In this situation, the host should process the following flow:

If (Tx Ready ==1)

This equality means that the logical address has been occupied by another CEC device. The host should give up this logical address and try another logical address.

Else if (Tx Retry Timeout ==1)

If (Tx Nack Counter == Tx Retry +1)

This means that the logical address is an available address and can be allocated to the device containing the HDMI Tx.

Else

This means the CEC Tx transmission has failed (Tx Retry +1) times – because either the initiator has detected NO ACK or a follower on the CEC bus has responded with a "low drive" error.. In this situation, the host needs to keep this logical address and try it again later.

Step 4
After confirming one of the three interrupts has occurred, Tx Enable has to be cleared, by writing '0' to 0x11[0], to prepare for the next transmission.

4.9.4.2 CEC Acts as a Follower:

Step 1
The host is ready to accept CEC messages on power-up.

Step 2

The CEC module will always monitor the CEC bus and accept broadcast messages or directly addressed messages. When any message besides a polling message is completely buffered in one of the CEC Rx Buffers, the CEC Receiver module will assert the corresponding CEC Rx Buffer Ready bit(0x49[2:0]) and the CEC Rx Buffer Ready Interrupt (0x97[2:0] Main map) bit will be asserted. The order of arrival of a new frame in each buffer is assigned to three two-bit timestamp registers (0x96[5:0]). Each timestamp register can assume a value between and including 0b01 and 0b11, depending on when a new frame arrives at the corresponding CEC Rx Buffer. A value of 0b01 corresponds to the earliest arrived message and a value of 0b11 corresponds to the latest.

Step 3
The host responds to the Rx Ready interrupt, and the CEC message in the received buffer will be read out from CEC module and delivered to the high-level software functions.

Step 4

After the interrupt handler has completed, the host system must clear the interrupt by setting the value of the corresponding CEC Rx Buffer Ready Interrupt Clear (0x97[2:0] Main map) to '1'. It must then toggle the CEC Rx Buffer Ready Clear (0xBA[2:0]) bit, which will clear the CEC Rx Buffer Ready (0xB9[2:0]) and also reset the value of the respective timestamp to '0'. Timestamp registers will be updated on arrival of a new data frame.

4.9.5 CEC System Control

4.9.6 CEC System Power and CDC Control

There is power-down bit, CEC PD, at register 0xE2 bit 0 in the main register map. This bit will reset all CEC logic and the CEC I2C map. Note that if CEC is powered down then the CEC can no longer respond to CEC commands. Refer to the "Additional Power Reduction Methods" section ► 4.8.2 for more details on the use of this bit.

The CEC Power Mode can be controlled by register bits 0x4E[1:0]. It can be always active, always powered down, or depend on the status of HPD. To reset the CEC registers Soft Reset (0x50[0]), can be set to 1, then back to 0.

HDMI 1.4 defines special Capability Discover and Control message arbitration rules. These rules are enabled by default, and can be disabled by setting the CDC Arbitration Enable register bit 0xF7[7] to 0. To automatically detect CDC messages the Physical Address must be written in registers 0x80 and 0x81.

4.9.7 CEC Timing Control

The CEC module requires an input clock from 3MHz to 100MHz, the timing registers and clock divider need to be adjusted based on the frequency of the input clock. The default settings for these registers are for a 12MHz input clock. If using an alternate frequency, refer to the "CEC Clock Timing Calculator" spreadsheet, which can be obtained by contacting ►ATV_VideoTx_Apps@analog.com. CEC timing register settings for the use of 3MHz, 13.5MHz, and 27MHz are provided in ► Table 105, ► Table 106, and ► Table 107.

Table 105 CEC Clock Timing Register Settings (CEC Memory Map) for 3MHz CEC Clock

Register	Name	Target Value	Target (uS)	Calculated Value (decimal)	Calculated Value (hex)	Register Setting (hex)
0x4E[7:2]	CEC Clock Divider	750KHz	1.33	3	0003	**00**
0x51	st_total	4.5ms	4500	3375	0D2F	**0D**
0x52						**2F**
0x53	st_total_min	4.2ms	4200	3150	0C4E	**0C**
0x54						**4E**
0x55	st_total_max	4.8ms	4800	3600	0E10	**0E**
0x56						**10**
0x57	st_low	3.7ms	3700	2775	0AD7	**0A**
0x58						**D7**
0x59	st_low_min	3.4ms	3400	2550	09F6	**09**
0x5A						**F6**
0x5B	st_low_max	4.0ms	4000	3000	0BB8	**0B**
0x5C						**B8**
0x5D	bit_total	2.4ms	2400	1800	0708	**07**
0x5E						**08**
0x5F	bit_total_min	1.95ms	1950	1463	05B7	**05**
0x60						**B7**
0x61	bit_total_max	2.85ms	2850	2138	085A	**08**
0x62						**5A**
0x63	bit_low_one	0.6ms	600	450	01C2	**01**
0x64						**C2**
0x65	bit_low_zero	1.5ms	1500	1125	0465	**04**
0x66						**65**
0x67	bit_low_max	1.8ms	1800	1350	0546	**05**
0x68						**46**
0x69	sample_time	1.05ms	1050	788	0314	**03**
0x6A						**14**
0x6B	line_error_time	3.6ms	3600	2700	0A8C	**0A**
0x6E						**8C**
0x6F	rise_time	250us	250	188	00BC	**00**
0x70						**BC**
0x71	bit_low_one_min	0.3ms	300	225	00E1	**00**
0x72						**E1**
0x73	bit_low_one_max	0.9ms	900	675	02A3	**02**
0x74						**A3**
0x75	bit_low_zero_min	1.2ms	1200	900	0384	**03**
0x76						**84**

Table 106 **CEC Clock Timing Register Settings (CEC Memory Map) for 13.5MHz CEC Clock**

Register	Name	Target Value	Target (uS)	Calculated Value (decimal)	Calculated Value (hex)	Register Setting (hex)
0x4e	clock_divider	750KHz	1.33	17	11	**11**
0x51	st_total	4.5ms	4500	3375	0D2F	**0D**
0x52						**2F**
0x53	st_total_min	4.2ms	4200	3150	0C4E	**0C**
0x54						**4E**
0x55	st_total_max	4.8ms	4800	3600	0E10	**0E**
0x56						**10**
0x57	st_low	3.7ms	3700	2775	0AD7	**0A**
0x58						**D7**
0x59	st_low_min	3.4ms	3400	2550	09F6	**09**
0x5a						**F6**
0x5b	st_low_max	4.0ms	4000	3000	0BB8	**0B**
0x5c						**B8**
0x5d	bit_total	2.4ms	2400	1800	0708	**07**
0x5e						**08**
0x5f	bit_total_min	1.95ms	1950	1463	05B7	**05**
0x60						**B7**
0x61	bit_total_max	2.85ms	2850	2138	085A	**08**
0x62						**5A**
0x63	bit_low_one	0.6ms	600	450	01C2	**01**
0x64						**C2**
0x65	bit_low_zero	1.5ms	1500	1125	0465	**04**
0x66						**65**
0x67	bit_low_max	1.8ms	1800	1350	0546	**05**
0x68						**46**
0x69	sample_time	1.05ms	1050	788	0314	**03**
0x6a						**14**
0x6b	line_error_time	3.6ms	3600	2700	0A8C	**0A**
0x6c						**8C**
0x6e	rise_time	250us	250	188	00BC	**00**
0x6f						**BC**
0x71	bit_low_one_min	0.3ms	300	225	00E1	**00**
0x72						**E1**
0x73	bit_low_one_max	0.9ms	900	675	02A3	**02**
0x74						**A3**
0x75	bit_low_zero_min	1.2ms	1200	900	0384	**03**
0x76						**84**

Table 107 **CEC Clock Timing Register Settings (CEC Memory Map) for 27MHz CEC Clock**

Register	Name	Target Value	Target (uS)	Calculated Value (decimal)	Calculated Value (hex)	Register Setting (hex)
0x4e	clock_divider	750KHz	1.33	35	23	23
0x51	st_total	4.5ms	4500	3375	0D2F	0D
0x52						2F
0x53	st_total_min	4.2ms	4200	3150	0C4E	0C
0x54						4E
0x55	st_total_max	4.8ms	4800	3600	0E10	0E
0x56						10
0x57	st_low	3.7ms	3700	2775	0AD7	0A
0x58						D7
0x59	st_low_min	3.4ms	3400	2550	09F6	09
0x5a						F6
0x5b	st_low_max	4.0ms	4000	3000	0BB8	0B
0x5c						B8
0x5d	bit_total	2.4ms	2400	1800	0708	07
0x5e						08
0x5f	bit_total_min	1.95ms	1950	1463	05B7	05
0x60						B7
0x61	bit_total_max	2.85ms	2850	2138	085A	08
0x62						5A
0x63	bit_low_one	0.6ms	600	450	01C2	01
0x64						C2
0x65	bit_low_zero	1.5ms	1500	1125	0465	04
0x66						65
0x67	bit_low_max	1.8ms	1800	1350	0546	05
0x68						46
0x69	sample_time	1.05ms	1050	788	0314	03
0x6a						14
0x6b	line_error_time	3.6ms	3600	2700	0A8C	0A
0x6c						8C
0x6e	rise_time	250us	250	188	00BC	00
0x6f						BC
0x71	bit_low_one_min	0.3ms	300	225	00E1	00
0x72						E1
0x73	bit_low_one_max	0.9ms	900	675	02A3	02
0x74						A3
0x75	bit_low_zero_min	1.2ms	1200	900	0384	03
0x76						84

Table 108 CEC System Control Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x92	R/W	[7]	0*******	Wake Up Opcode8 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode8 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[6]	*0******	Wake Up Opcode7 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode7 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[5]	**0*****	Wake Up Opcode6 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode6 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[4]	***0****	Wake Up Opcode5 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode5 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[3]	****0***	Wake Up Opcode4 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode4 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[2]	*****0**	Wake Up Opcode3 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode3 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[1]	******0*	Wake Up Opcode2 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode2 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[0]	*******0	Wake Up Opcode1 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode1 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
0x93	R/W	[7]	0*******	Wake Up Opcode8 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode8 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[6]	*0******	Wake Up Opcode7 Interrupt	CEC Wake Up Code Interrupt Enable interrupt detecting Wake Up Opcode7 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[5]	**0*****	Wake Up Opcode6 Interrupt	CEC Wake Up Code Interrupt Enable Interrupt detecting Wake Up Opcode6 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected

Address	Type	Bits	Default Value	Register Name	Function
		[4]	***0****	Wake Up Opcode5 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode5 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[3]	****0***	Wake Up Opcode4 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode4 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[2]	*****0**	Wake Up Opcode3 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode3 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[1]	******0*	Wake Up Opcode2 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode2 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[0]	*******0	Wake Up Opcode1 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode1 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
0xE2	R/W	[0]	*******0	CEC Power Down	CEC Power Down Power down CEC logic and reset CEC I2C map 0 = disabled 1 = enabled

Table 109 CEC System Control Related Registers (CEC Map)

Address	Type	Bits	Default Value	Register Name	Function
0x4B	R/W	[6:4]	*001****	Logical Address Mask	Logical Address Mask of the CEC Devices: Supports up to 3 logical devices. When the bit is one, the related logical device will be enabled, and the messages whose destination address is matched with the logical address will be accepted 001 = mask bit for logical device0 010 = mask bit for logical device1 100 = mask bit for logical device2
		[3]	****0***	Error Report Mode	Error report mode 0 = only report short bit period error 1 = report both short and long bit period errors
		[2]	*****0**	Error Detect Mode	Error Detect Mode If an error is detected, CEC controller will drive the CEC line low for 3.6msec immediately to notify the line error to the initiator 0 = any short bit period except start bit 1 = only when destination is broadcast
		[1]	******0*	Force NACK	Force NACK. If this bit is set, CEC Rx module will NACK any message. 0 = ACK the relevant messages 1 = NACK all messages
		[0]	*******0	Force Ignore	If this bit is set, CEC Rx module will ignore any directly addressed message belonging to it. 0 = ACK the relevant messages 1 = NACK all messages
0x4C	R/W	[7:4]	1111****	Logical Address 1	Logical Address of logical device 1
		[3:0]	****1111	Logical Address 0	Logical Address of logical device 0
0x4D	R/W	[3:0]	****1111	Logical Address 2	Logical Address of logical device 2
0x4E	R/W	[7:2]	001111**	CEC Clock Divider	CEC Clock Divider: The input clock frequency is divided according to the value in this register. The divided clock is used as the CEC process clock. Internal clock frequency = input clock frequency / (clock_divider+1) 000000 = no division and the input clock will be used as the CEC process clock directly 000001 = divide by 2 000010 = divide by 3 000011 = divide by 4 111110 = divide by 63 111111 = divide by 64
		[1:0]	******00	CEC Power Mode	Power mode of CEC. Does not reset I2C map on power down. 00 = Completely Power Down 01 = Always Active 10 = Depend on HPD status 11 = Depend on HPD status
0x4F	R/W	[5:0]	**000111	Glitch Filter	Glitch filter control for the CEC input: The CEC bus is sampled by the input clock.

Address	Type	Bits	Default Value	Register Name	Function
				Ctrl	This Register indicates the number of clock cycles. Pulses whose width is less than the value in this register will be filtered by the CEC module. 000000 = filter is disabled 000001 = pulse width less than 1 clock cycle will be filtered. 111111 = pulse width less than 63 will be filtered
0x50	R/W	[0]	*******0	CEC Soft Reset	CEC reset by external host 0 = Do not reset CEC controller 1 = Reset CEC controller
0x51	R/W	[15:0]	00001101	St Total	CEC nominal start bit total period. Typically it is 4.5ms Typical value at 750KHz
0x52			00101111		
0x53	R/W	[15:0]	00001100	St Total Min	CEC minimum start bit total period. Typically, it is 4.3ms, for the default value, keep 0.1ms margin, namely 4.2ms Typical value at 750KHz
0x54			01001110		
0x55	R/W	[15:0]	00001110	St Total Max	CEC maximum start bit total period. Typically, it is 4.7ms, for the default value, keep 0.1ms margin, namely 4.8ms Typical value at 750KHz
0x56			00010000		
0x57	R/W	[15:0]	00001010	St Low	CEC nominal start bit low period. Typically it is 3.7ms Typical value at 750KHz
0x58			11010111		
0x59	R/W	[15:0]	00001001	St Low Min	CEC minimum start bit low period. Typically it is 3.5ms, for the default value, keep 0.1ms margin, namely 3.4ms Typical value at 750KHz
0x5A			11110110		
0x5B	R/W	[15:0]	00001011	St Low Max	CEC maximum start bit low period. Typically it is 3.9ms, for the default value, keep 0.1ms margin, namely 4.0ms Typical value at 750KHz
0x5C			10111000		
0x5D	R/W	[15:0]	00000111	Bit Total	CEC nominal data bit total period. Typically it is 2.4ms. Typical value at 750KHz
0x5E			00001000		
0x5F	R/W	[15:0]	00000101	Bit Total Min	CEC minimum data bit low period. Typically it is 2.05ms, for the default value, keep 0.1ms margin, namely 1.95ms Typical value at 750KHz
0x60			10110111		
0x61	R/W	[15:0]	00001000	Bit Total Max	CEC maximum data bit low period. Typically it is 2.75ms, for the default value, keep 0.1ms margin, namely 2.85ms Typical value at 750KHz
0x62			01011010		
0x63	R/W	[15:0]	00000001	Bit Low One	CEC nominal data bit low period for logical 1. Typically it is 0.6ms Typical value at 750KHz
0x64			11000010		
0x65	R/W	[15:0]	00000100	Bit Low Zero	CEC nominal data bit low period for logical 0. Typically it is 1.5ms Typical value at 750KHz
0x66			01100101		
0x67	R/W	[15:0]	00000101	Bit Low Max	CEC nominal data bit low period for logical 0. Typically it is 1.8ms

Address	Type	Bits	Default Value	Register Name	Function
0x68			01000110		Typical value at 750KHz
0x69	R/W	[15:0]	00000011	Sample Time	CEC nominal sample time. Typically it is 1.05ms Typical value at 750KHz
0x6A			00010011		
0x6B	R/W	[15:0]	00001010	Line Error Time	CEC Line Error handling time. Typically it is 1.4~1.6 times the nominal data bit period. We set the default value to 1.5 times the nominal data bit period.
0x6C			10001100		
0x6E	R/W	[15:0]	00000000	Rise Time	CEC maximum rise time. Typically it is 250us
0x6F			10111100		
0x70	R/W	[0]	*******0	Bit Low Detmode	Error detection mode for data bit low period 0 = Disabled 1 = Enable
0x71	R/W	[15:0]	00000000	Bit Low One Min	CEC minimum data bit low period for logical 1. Typically it is 0.4ms, for the default value, keep 0.1ms margin, namely 0.3ms Typical value at 750KHz
0x72			11100001		
0x73	R/W	[15:0]	00000010	Bit Low One Max	CEC maximum data bit low period for logical 1. Typically it is 0.8ms, for the default value, keep 0.1ms margin, namely 0.9ms Typical value at 750KHz
0x74			10100011		
0x75	R/W	[15:0]	00000011	Bit Low Zero Min	CEC minimum data bit low period for logical 0. Typically it is 1.3ms, for the default value, keep 0.1ms margin, namely 1.2ms Typical value at 750KHz
0x76			10000100		
0x77	R/W	[7:0]	01101101	Wake Up Opcode 1	Wake up opcode 0 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Power On' opcode
0x78	R/W	[7:0]	10001111	Wake Up Opcode 2	Wake up opcode 1 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Give Power Status' opcode
0x79	R/W	[7:0]	10000010	Wake Up Opcode 3	Wake up opcode 2 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Active Source' opcode
0x7A	R/W	[7:0]	00000100	Wake Up Opcode 4	Wake up opcode 3 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Image View On' opcode
0x7B	R/W	[7:0]	00001101	Wake Up Opcode 5	Wake up opcode 4 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-

Address	Type	Bits	Default Value	Register Name	Function
					define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Text View On' opcode
0x7C	R/W	[7:0]	01110000	Wake Up Opcode 6	Wake up opcode 5 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'System Audio Mode Request' opcode
0x7D	R/W	[7:0]	01000010	Wake Up Opcode 7	Wake up opcode 6 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Deck Control' opcode
0x7E	R/W	[7:0]	01000001	Wake Up Opcode 8	Wake up opcode 7 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Play' opcode
0x7F	R/W	[7]	1*******	CDC Arbitration Enable	Controls whether to do special CDC message arbitration upon receiving CDC message 1 = enable 0 = disable
		[6]	*1******	CDC HPD Response Enable	Controls whether to toggle internal HPD signals when receiving CDC HPD message 1 = enable 0 = disable
0x80	R/W	[15:0]	00000000	CEC Physical Address	Physical address of CEC device
0x81			00000000		
0x82	R/W	[7:0]	00000001	CDC HPD Timer Count	Controls the time CDC HPD stays low when receiving CDC HPD toggle message. HPD low = CDC_HPD_Timer_Count * CEC_CLK. CEC_CLK is 760KHz by default.
0x83	RO	[7]	0*******	CDC HPD	HPD signal from CEC interface

4.10 HDCP/EDID Controller

4.10.1 ADV7511 EDID/HDCP Support Features

The ADV7511's EDID and DDC Controllerperforms three main functions to support the system's EDID and HDCP handling. These features are outlined below. A block diagram is illustrated in ► Figure 33.

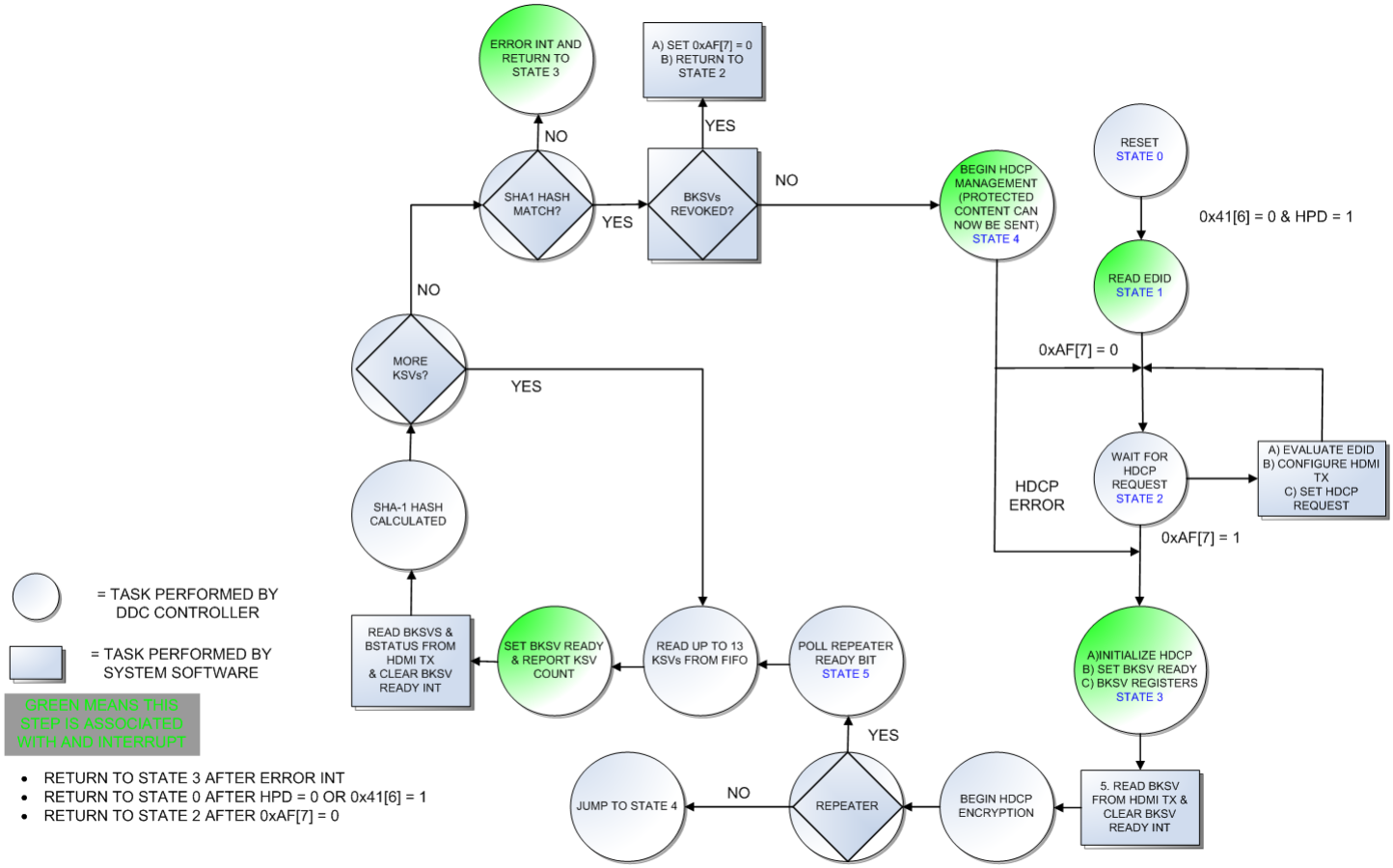
- Reads EDID segment 0 from the display as soon as Hot Plug is detected and the chip is set to powered up mode.
  - The 256-byte EDID segment is stored in internal RAM and can be read via I2C and has its own I2C address. The I2C slave address of the EDID memory can be programmed in the EDID ID register (0x43). The default value for this register is 0x7E.
  - Reads additional EDID segments on demand.

- These segments are stored in the same location as the first segment. Therefore, the controller should store the first segment prior to initializing another EDID segment download.

- Implements the HDCP transmitter state machine including handling of downstream repeaters.
- Includes robust error reporting to report various error conditions to the system firmware.

► Figure 33 shows a flow chart of the State Machine implemented by the internal controller. Circles indicate functions that are controlled automatically within the ADV7511, and squares indicate functions that must be implemented in the system software.

Figure 33 ADV7511 EDID and DDC Controller Functional Flow



4.11 Interrupt Handling

The ADV7511 has interrupts to help with the system design. The interrupts allow the internal HDCP/EDID controller to alert the system of the events listed in ► Table 110. For Hot Plug Detect and Monitor Sense, the interrupt will be triggered for every transition, so the read-only register must be used to determine if the HPD or Monitor Sense is logic high or logic low.

Table 110 Interrupt Handling Registers

Interrupt	Interrupt Register	Related Registers	Mask Register
Wake Up Opcode 1	0x93[7]	0x77 (CEC Map)	0x92[7]
Wake Up Opcode 2	0x93[6]	0x78 (CEC Map)	0x92[6]
Wake Up Opcode 3	0x93[5]	0x79 (CEC Map)	0x92[5]
Wake Up Opcode 4	0x93[4]	0x7A (CEC Map)	0x92[4]
Wake Up Opcode 5	0x93[3]	0x7B (CEC Map)	0x92[3]
Wake Up Opcode 6	0x93[2]	0x7C (CEC Map)	0x92[2]
Wake Up Opcode 7	0x93[1]	0x7D (CEC Map)	0x92[1]
Wake Up Opcode 8	0x93[0]	0x7E (CEC Map)	0x92[0]
Hot Plug Detect	0x96[7]	0x42[6]	0x94[7]
Monitor Sense	0x96[6]	0x42[5]	0x94[6]
Active Vsync Edge	0x96[5]	N/A	0x94[5]
Audio FIFO full	0x96[4]	N/A	0x94[4]
Embedded Sync Parity Error	0x96[3]	N/A	0x94[3]
EDID Ready	0x96[2]	EDID Memory Map	0x94[2]
HDCP Authenticated	0x96[1]	0xC8[3:0]	0x94[1]
HDCP Error	0x97[7]	0xC8[7:4]	0x95[7]
BKSV Flag	0x97[6]	0xBF – 0xC3 and EDID Memory Map	0x95[6]
CEC Tx ready	0x97[5]	N/A	0x95[5]
CEC Tx arbitration lost	0x97[4]	N/A	0x95[4]
CEC Tx retry timeout	0x97[3]	N/A	0x95[3]
CEC Rx ready 3	0x97[2]	0x38 – 0x48 (CEC Map)	0x95[2]
CEC Rx ready 2	0x97[1]	0x27 – 0x37 (CEC Map)	0x95[1]
CEC Rx ready 1	0x97[0]	0x15 - 0x25 (CEC Map)	0x95[0]

4.11.1 Wake Up Opcodes

The Wake UpOpcode interrupts correspond to registers 0x77 – 0x7E in the CEC register map. When a user defined opcode is detected in an incoming CEC message, the corresponding interrupt will be triggered.

4.11.2 Hot Plug Detect

This interrupt is triggered every time there is an HPD transition from high to low or low to high.

4.11.3 Monitor Sense

This interrupt is triggered every time the TMDS clock line voltages both cross 1.8V from high to low or low to high.

4.11.4 Active Vsync Edge

This interrupt is triggered whenever ADV7511 detects a Vsync leading edge. This applies to all input types. Vsync edge detection is useful for timing some I2C writes such as enabling CSC and Gamut Metadata Packet information. See the following sections for further information:

- 4.3.8.3 - Changing the Color Space with Active Display
- 4.3.9.3 - Gamut Metadata Packet

4.11.5 Audio FIFO Full

This interrupt is triggered if more data goes into the audio FIFO than comes out. If it happens at initialization period, it is not a problem. If it happens after the system is fully configured, then there is a problem with the system.

4.11.6 Embedded Sync Parity Error

This interrupt is triggered when the embedded sync parity protection encounters two errors in F/V/H bits of EAV or SAV bits. ADV7511 is able to correct a one-bit error and flag a two-bit error.

4.11.7 EDID Ready

This interrupt is triggered when the EDID has been read from the receiver and is available in the ADV7511 EDID memory to be read at I2C address 0x7E (programmable). If the EDID Ready flag does not occur after EDID is expected, an I2C Error on the HDCP Error interrupt will occur if enabled.

4.11.8 HDCP Authenticated

This interrupt occurs when the HDCP/EDID state machine transitions from state 3 to state 4. This means that the final BKSV flag has been cleared and the host system has access to all of the downstream BKSVs. This means that authentication is complete and it is now safe for the host to send copyrighted audio and video data across the HDCP-protected HDMI link.

4.11.9 HDCP Error

This interrupt is triggered when the HDCP/EDID Controller is reporting an error to the system software. The error which occurred is represented by an error code contained in I2C register 0xC8[7:4].

4.11.10 BKSV Flag

This interrupt is triggered when KSVs from a downstream device are read into the ADV7511. If the BKSV count register (0xC7[6:0]) is zero, then the 5 byte KSV from the receiver directly connected to the ADV7511 will be available in registers 0xBF – 0xC3. If the BKSV count register 1 or greater, then the specified amount of 5 byte KSVs from downstream devices will be available in the EDID memory.

4.11.11 CECTx Ready Flag

This interrupt indicates that the CEC host is ready to transmit data.

4.11.12 CECTx Arbitration Lost Flag

This interrupt reflects the fact that the Tx was trying to transmit but lost a bus arbitration to another CEC device.

4.11.13 CECTx Retry Timeout Flag

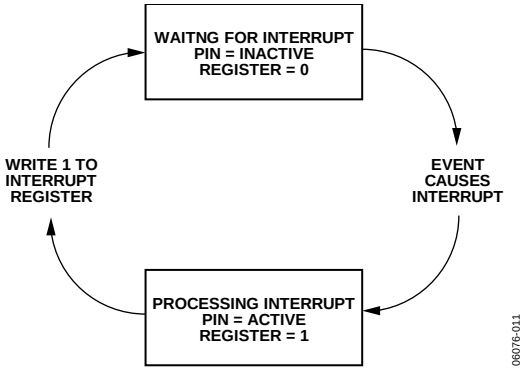
This interrupt indicates that the Tx retried in excess of the limit programmed into the Tx_retry register (0x12[6:4]) of the CEC memory block.

4.11.14 CEC Rx Ready Flags

This interrupt indicates that the CEC host is ready to monitor and receive data for a corresponding CEC Buffer.

►147Figure 34 shows the process of detecting and clearing an interrupt. The interrupt pin and interrupt register become active simultaneously when an event triggers an interrupt. The system software processes the interrupt, and then writes a '1' to the interrupt register to clear the register and set the interrupt pin back to inactive. The pin will remain active until each active interrupt register is cleared.

Figure 34 Interrupt Handling



Masks are available to let the user selectively activate each interrupt. To enable a specific interrupt register, write 1 to the corresponding mask bit. The mask bits will not affect the interrupt registers, only the interrupt pin. For some interrupts there are read-only registers available for checking the state.

► Figure 35 shows a recommended flow for processing ADV7511 interrupts.

Figure 35 Interrupt Handling Example

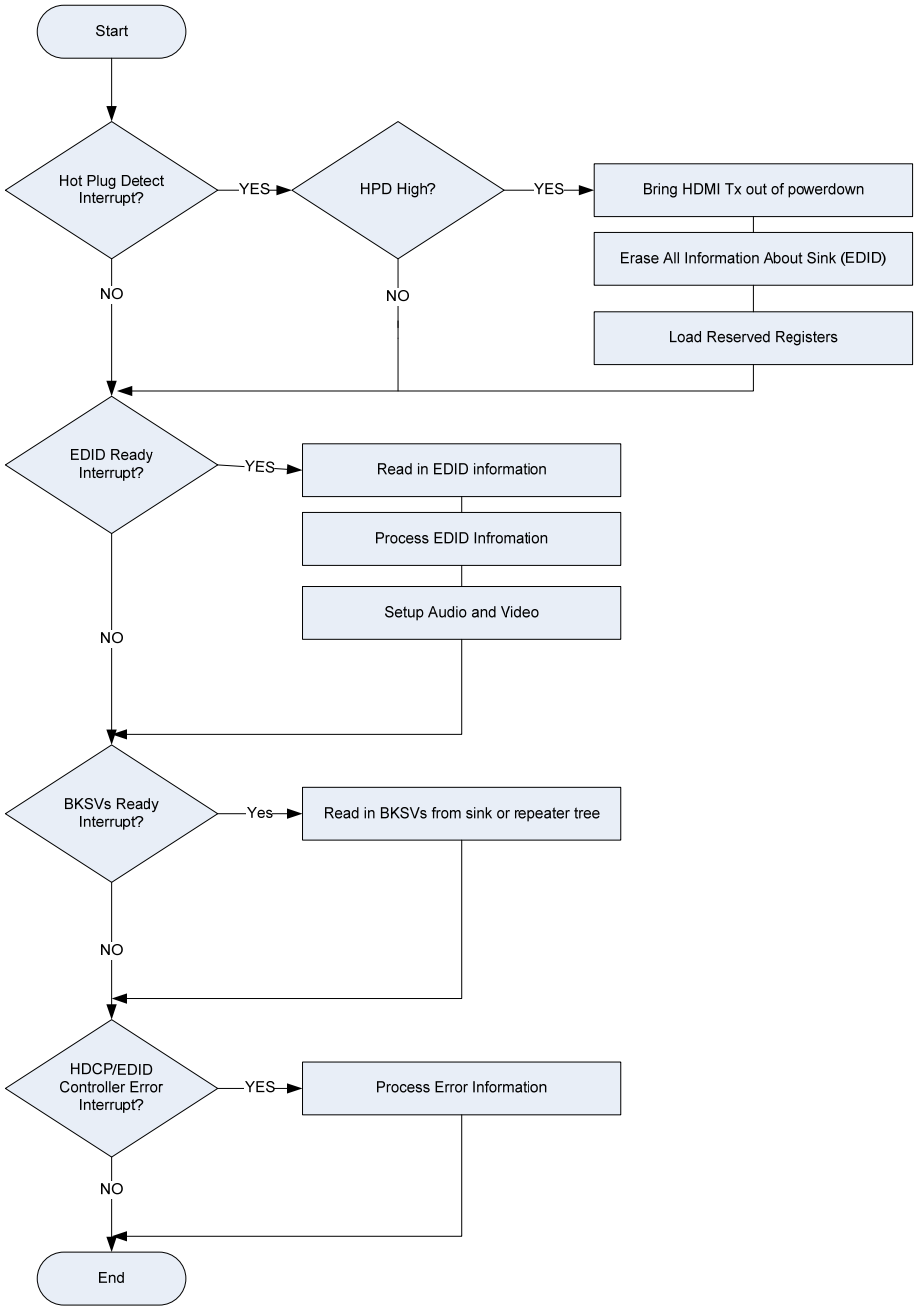


Table 111 Interrupt Handling Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0x92	R/W	[7]	0*******	Wake Up Opcode 1 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 1 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[6]	*0******	Wake Up Opcode 2 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 2 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[5]	**0*****	Wake Up Opcode 3 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 3 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[4]	***0****	Wake Up Opcode 4 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 4 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[3]	****0***	Wake Up Opcode 5 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 5 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[2]	*****0**	Wake Up Opcode 6 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 6 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[1]	******0*	Wake Up Opcode 7 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 7 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
		[0]	*******0	Wake Up Opcode 8 Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode 8 in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled
0x93	R/W	[6]	*0******	Wake Up Opcode 2 Interrupt	CEC Wake Up Code Interrupt Enable interrupt detecting Wake Up Opcode 2 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[5]	**0*****	Wake Up Opcode 3 Interrupt	CEC Wake Up Code Interrupt Enable Interrupt detecting Wake Up Opcode 3 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[4]	***0****	Wake Up Opcode 4 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 4 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[3]	****0***	Wake Up Opcode 5 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 5 in CEC message 0= No Interrupt Detected

Address	Type	Bits	Default Value	Register Name	Function
					1 = Interrupt Detected
		[2]	*****0**	Wake Up Opcode 6 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 6 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[1]	******0*	Wake Up Opcode 7 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 7 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
		[0]	*******0	Wake Up Opcode 8 Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode 8 in CEC message 0= No Interrupt Detected 1 = Interrupt Detected
0x94	R/W	[7]	1*******	HPD Interrupt Enable	HPD Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[5]	**0*****	Vsync Interrupt Enable	Vsync Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[4]	***0****	Audio FIFO Full Interrupt Enable	Audio FIFO Full Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[2]	*****0**	EDID Ready Interrupt Enable	EDID Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[1]	******0*	HDCP Authenticated Interrupt Enable	HDCP Authenticated Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x95	R/W	[7]	0*******	DDC Controller Error Interrupt Enable	DDC Controller Error Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[6]	*0******	BKSV Flag Interrupt Enable	BKSV Flag Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[5]	**0*****	Tx Ready Interrupt Enable	Tx Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[4]	***0****	Tx Arbitration Lost Interrupt Enable	Tx Arbitration Lost Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[3]	****0***	Tx Retry Timeout Interrupt Enable	Tx Retry Timeout Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[2]	*****0**	Rx Ready 3 Interrupt Enable	Rx Ready 3 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled

Address	Type	Bits	Default Value	Register Name	Function
		[1]	******0*	Rx Ready 2 Interrupt Enable	Rx Ready 2 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
		[0]	*******0	Rx Ready 1 Interrupt Enable	Rx Ready 1 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled
0x96	R/W	[7]	0*******	HPD Interrupt	HPD Interrupt 0 = no interrupt detected 1 = interrupt detected
		[5]	**0*****	Vsync Interrupt	Vsync Interrupt 0 = no interrupt detected 1 = interrupt detected
		[4]	***0****	Audio FIFO Full Interrupt	Audio FIFO Full Interrupt 0 = no interrupt detected 1 = interrupt detected
		[2]	*****0**	EDID Ready Interrupt	EDID Ready Interrupt 0 = no interrupt detected 1 = interrupt detected
		[1]	******0*	HDCP Authenticated	HDCP Authenticated 0 = no interrupt detected 1 = interrupt detected
		[0]	*******0	Fixed @ 0b	Reserved
0x97	R/W	[7]	0*******	DDC Controller Error Interrupt	DDC Controller Error Interrupt 0 = no interrupt detected 1 = interrupt detected
		[6]	*0******	BKSV Flag Interrupt	BKSV Flag Interrupt 0 = no interrupt detected 1 = interrupt detected
		[5]	**0*****	Tx Ready Interrupt	Tx Ready Interrupt 0 = no interrupt detected 1 = interrupt detected
		[4]	***0****	Tx Arbitration Lost Interrupt	Tx Arbitration Lost interrupt 0 = no interrupt detected 1 = interrupt detected
		[3]	****0***	Tx Retry Timeout Interrupt	Tx Retry Timeout interrupt 0 = no interrupt detected 1 = interrupt detected
		[2]	*****0**	Rx Ready 3 Interrupt	Rx Ready 3 Interrupt 1 = interrupt detected for rx buffer 3 0 = no interrupt detected for buffer 3 1 = interrupt detected for buffer 3 0 = no interrupt detected for buffer 3
		[1]	******0*	Rx Ready 2 Interrupt	Rx Ready 2 Interrupt 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2

Address	Type	Bits	Default Value	Register Name	Function
		[0]	*******0	Rx Ready 1 Interrupt	Rx Ready 1 Interrupt 1 = interrupt detected for rx buffer 1 0 = no interrupt detected for buffer 1 1 = interrupt detected for buffer 1 0 = no interrupt detected for buffer 1
0xA1	R/W	[6]	*0******	Monitor Sense Power Down	Monitor Sense Power Down 0 = Monitor Sense monitoring enabled 1 = Monitor Sense monitoring disabled

SECTION 5 - REGISTER MAPS

The ADV7511 contains four 256-byte register maps as described in section ► 4.1. The full details of each relevant address byte is described in the following section. For each register map, addresses between 0x00 and 0xFF not included in the register map are not affected by I2C writes and will always read '0'. The far right column of the following tables contain a linked reference to the Programming Guide section that provides more detail as to the operation of the particular register being described.

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
0x00	RO	[7:0]	00010010	Chip Revision	Revision of the chip	
0x01	R/W	[19:0]	****0000	N	20 bit N used with CTS to regenerate the audio clock in the receiver.	4.4.2
0x02			00000000			
0x03			00000000			
0x04	RO	[7:4]	0000****	SPDIF Sampling Frequency	SPDIF Sampling Frequency from SPDIF Channel Status. 0000 = 44.1 kHz 0001 = N/A 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = N/A 0101 = N/A 0110 = N/A 0111 = N/A 1000 = 88.2 kHz 1001 = N/A 1010 = 96.0 kHz 1011 = N/A 1100 = 176.4 kHz 1101 = N/A 1110 = 192.0 kHz 1111 = N/A	4.4.1
0x04	RO	[19:0]	****0000	CTS Automatic	Cycle Time Stamp (CTS) Automatically Generated This 20 bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits see 0x05 and 0x06.	4.4.2
0x05			00000000			
0x06			00000000			
0x07	R/W	[19:0]	****0000	CTS Manual	Cycle Time Stamp (CTS) Manually Entered This 20 bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits see 0x08 and 0x09.	4.4.2
0x08			00000000			
0x09			00000000			
0x0A	R/W	[7]	0*******	CTS Select	CTS Source Select. 0 = CTS Automatic 1 = CTS Manual	4.4.2
		[6:4]	*000****	Audio Select	Audio Select All others invalid 000 = I2S 001 = SPDIF 010 = One Bit Audio (DSD) 011 = High Bit Rate (HBR Audio) 100 = DST 101 = N/A	4.4.1 4.4.1.1 4.4.1.3 4.4.1.4 4.4.1.5

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					110 = N/A 111 = N/A	
		[3:2]	****00**	Audio Mode	Mode Selection for Audio Select Case 1: DSD (Audio Select register bits (0x0A[6:4] = 0b010)) 0X = DSD raw mode 1X = SDIF-3 mode Case 2: HBR (Audio Select register bits (0x0A[6:4] = 0b011)) 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding Case 3: DST (Audio Select register bits (0x0A[6:4] = 0b100)) X0 = normal mode 01 = 2x clock 11 = 1x clock or DDR case 00 = 4 stream, with BPM encoding 01 = 4 stream, no BPM encoding 10 = 1 stream, with BPM encoding 11 = 1 stream, no BPM encoding	4.4.1 4.4.1.1 4.4.1.3 4.4.1.4 4.4.1.5
		[1:0]	******01	MCLK Ratio	MCLK Ratio The ratio between the audio sampling frequency and the clock described using N and CTS 00 = 128xfs 01 = 256xfs 10 = 384xfs 11 = 512xfs	4.4.1
0x0B	R/W	[7]	0*******	SPDIF Enable	Enable or Disable SPDIF receiver 0 = disable 1 = Enabled	4.4.1
		[6]	*0******	Audio Clock Polarity	SPDIF MCLK, I2S SCLK, and DSD Clock Polarity Indicates edge where input data is latched 0 = rising edge 1 = falling edge	4.4.1
		[5]	**0*****	MCLK Enable	MCLK Enable 0 = MCLK internally generated 1 = MCLK is available	4.4.1
		[4:1]	***0111*	Fixed	Must be set to Default Value	
0x0C	R/W	[7]	1*******	Audio Sampling Frequency Select	Select source of audio sampling frequency for pixel repeat and I2S mode 4 0 = use sampling frequency from I2S stream 1 = use sampling frequency from I2C register	4.4.1
		[6]	*0******	Channel Status Override	Source of channel status bits when using I2S mode 4 0 = use channel status bits from I2S stream 1 = use channel status bits from I2C registers	4.4.1
		[5]	**1*****	I2S3 Enable	I2S3 enable for the I2S 3 pin. 0 = Disabled 1 = Enabled	4.4.1
		[4]	***1****	I2S2 Enable	I2S2 enable for the I2S 2 pin.	4.4.1

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					0 = Disabled 1 = Enabled	
		[3]	****1***	I2S1 Enable	I2S1 enable for the I2S 1 pin. 0 = Disabled 1 = Enabled	4.4.1
		[2]	*****1**	I2S0 Enable	I2S0 enable for the I2S 0 pin. 0 = Disabled 1 = Enabled	4.4.1
		[1:0]	******00	I2S Format	I2S Format 00 = Standard I2S mode 01 = right justified mode 10 = left justified mode 11 = AES3 direct mode	4.4.1
0x0D	R/W	[4:0]	***11000	I2S Bit Width	I2S Bit Width For right justified audio only. Default is 24. Not valid for widths greater than 24.	4.4.1
0x0E	R/W	[5:3]	**000***	Subpacket 0 L Source	Source of sub packet 0, left channel	4.4.3
		[2:0]	*****001	Subpacket 0 R Source	Source of sub packet 0, right channel	4.4.3
0x0F	R/W	[5:3]	**010***	Subpacket 1 L Source	Source of sub packet 1, left channel	4.4.3
		[2:0]	*****011	Subpacket 1 R Source	Source of sub packet 1, right channel	4.4.3
0x10	R/W	[5:3]	**100***	Subpacket 2 L Source	Source of sub packet 2, left channel	4.4.3
		[2:0]	*****101	Subpacket 2 R Source	Source of sub packet 2, right channel	4.4.3
0x11	R/W	[5:3]	**110***	Subpacket 3 L Source	Source of sub packet 3, left channel	4.4.3
		[2:0]	*****111	Subpacket 3 R Source	Source of sub packet 3, right channel	4.4.3
0x12	R/W	[7]	0*******	Audio Sample Word (CS bit 1)	Audio Sample Word 0 = Audio sample word represents linear PCM samples 1 = Audio sample word used for other purposes Consumer Use Should be 0 for HDMI	4.4.3
		[6]	*0******	Consumer Use (CS bit 0)	Consumer Use Bit 0 = Audio sample word represents linear PCM samples 1 = Audio sample word used for other purposes	4.4.3
		[5]	**0*****	Copyright Bit (CS bit 2)	Copy Right Bit 0 = Copyright Protected 1 = Not Copyright Protected	4.4.3
		[4:2]	***000**	Additional Audio Info (CS bits 5-3)	Additional information for Channel Status Bits 000 = 2 audio channels w/o pre-emphasis	4.4.3

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					001 = 2 audio channels with 50/15uS pre-emphasis 010 = Fixed 011 = Fixed	
		[1:0]	******00	Audio Clock Accuracy (CS bits 29-28)	Audio Clock Accuracy 00 = level II - normal accuracy +/-1000 X 10-6 10 = level III -variable pitch shifted clock 01 = level I - high accuracy +/-50 X 10-6 11 = Fixed	4.4.3
0x13	R/W	[7:0]	00000000	Category Code (CS bits 15-8)	Channel Status Category Code	4.4.3
0x14	R/W	[7:4]	0000****	Source Number (CS bits 19-16)	Channel Status Source Number	4.4.3
		[3:0]	****0000	Word Length (CS bits 35-32)	Audio Word Length 0000 = Not Specified 0001 = Not Specified 0010 = 16 Bits 0011 = 20 Bits 0100 = 18 Bits 0101 = 22 Bits 0110 = No description 0111 = No description 1000 = 19 Bits 1001 = 23 Bits 1010 = 20 Bits 1011 = 24 Bits 1100 = 17 Bits 1101 = 21 Bits 1110 = No description 1111 = No description	4.4.3
0x15	R/W	[7:4]	0000****	I2S Sampling Frequency (CS bits 27-24)	Sampling frequency for I2S audio. This information is used by both the audio Rx and the pixel repetition. 0000 = 44.1 kHz 0001 = Do not use 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = Do not use 0101 = Do not use 0110 = Do not use 0111 = Do not use 1000 = 88.2 kHz 1001 = HBR Audio 1010 = 96.0 kHz 1011 = Do not use 1100 = 176.4 kHz 1101 = Do not use 1110 = 192.0 kHz 1111 = Do not use	4.4.3
		[3:0]	****0000	Input ID	Input Video Format See ►Table 16to ►Table 27 0000 = 24 bit RGB 4:4:4 or YCbCr 4:4:4 (separate syncs) 0001 = 16, 20, 24 bit YCbCr 4:2:2 (separate syncs)	4.3.1

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					0010 = 16, 20, 24 bit YCbCr 4:2:2 (embedded syncs) 0011 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, separate syncs) 0100 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, embedded syncs) 0101 = 12, 15, 16 bit RGB 4:4:4 or YCbCr (DDR with separate syncs) 0110 = 8,10,12 bit YCbCr 4:2:2 (DDR with separate syncs) 0111 = 8, 10, 12 bit YCbCr 4:2:2 (DDR separate syncs) 1000 = 8, 10, 12 bit YCbCr 4:2:2 (DDR embedded syncs)	
0x16	R/W	[7]	0*******	Output Format	Output Format 0 = 4:4:4 1 = 4:2:2	4.3.1
		[6]	*0******	Reserved	Must be set to Default Value	
		[5:4]	**00****	Color Depth	Color Depth for Input Video Data. See ►Table 16 to ►Table 27 00 = invalid 10 = 12 bit 01 = 10 bit 11 = 8 bit	4.3.1
		[3:2]	****00**	Input Style	Styles refer to the input pin assignments. See ►Table 16 to ►Table 27 00 = Not Valid 01 = style 2 10 = style 1 11 = style 3	4.3.1
		[1]	******0*	DDR Input Edge	Video data input edge selection. Defines the first half of pixel data clocking edge. Used for DDR Input ID 5 and 6 only. 0 = falling edge 1 = rising edge	4.3.1
		[0]	*******0	Output Colorspace for Black Image	Input Color Space Selection Used for Black Image and Range Clipping 0 = RGB 1 = YCbCr	4.3.8
0x17	R/W	[7]	0*******	Fixed	Must be set to Default Value	
		[6]	*0******	Vsync Polarity	Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through 1 = sync polarity invert 0 = High polarity 1 = Low polarity	4.3.1
		[5]	**0*****	Hsync Polarity	HSync polarity for Embedded Sync Decoder and Sync Adjustment Case 1: Sync Adjustment Register (0x41[1]) = 1 0 = high polarity 1 = low polarity Case 2: Sync Adjustment Register (0x41[1]) = 0 0 = sync polarity pass through	4.3.1

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					1 = sync polarity invert 0 = High polarity 1 = Low polarity	
		[4:3]	***00***	Reserved @ 00b	Must be set to Default Value	
		[2]	*****0**	4:2:2 to 4:4:4 Interpolation Style	4:2:2 to 4:4:4 Up Conversion Method 0 = use zero order interpolation 1 = use first order interpolation	4.3.1
		[1]	******0*	Aspect Ratio	Aspect ratio of input video. 0 = 4:3 Aspect Ratio 1 = 16:9 Aspect Ratio	4.3.3
		[0]	*******0	DE Generator Enable	Enable DE Generator See registers 0x35 - 0x3A 0 = Disabled 1 = Enabled	4.3.7
0x18	R/W	[7]	0*******	CSC Enable	Color Space Converter Enable 0 = CSC Disabled 1 = CSC Enabled	4.3.8
		[6:5]	*10*****	CSC Scaling Factor	Color Space Converter Mode Sets the fixed point position of the CSC coefficients. Including the a4, b4, c4, offsets. 00 = +/- 1.0, -4096 - 4095 01 = +/- 2.0, -8192 - 8190 10 = +/- 4.0, -16384 - 16380 11 = +/- 4.0, -16384 - 16380	4.3.8
0x18	R/W	[12:0]	***00110	A1 (CSC)	Color space Converter (CSC) coefficient for equations: **Equation 1: CSC Channel A** $Out\_A = \left[In\_A\frac{A1}{4096} + In\_B\frac{A2}{4096} + In\_C\frac{A3}{4096} + A4 \right] 2^{CSC\_Mode}$ **Equation 2: CSC Channel B** $Out\_B = \left[In\_A\frac{B1}{4096} + In\_B\frac{B2}{4096} + In\_C\frac{B3}{4096} + B4 \right] 2^{CSC\_Mode}$ **Equation 3: CSC Channel C** $Out\_C = \left[In\_A\frac{C1}{4096} + In\_B\frac{C2}{4096} + In\_C\frac{C3}{4096} + C4 \right] 2^{CSC\_Mode}$	4.3.8
0x19			01100010			
0x1A	R/W	[5]	**0*****	Coefficient Update	There are 2 methods to update the coefficients. Method 1: When Coefficient Update is always 0, the coefficient will be updated directly. Method 2: When Coefficient Update is used, there are 3 steps for updating a) Set Coefficient Update = 1 to buffer the CSC Coefficients b) Set the new CSC Coefficients c) Set Coefficient Updated = 0 to enable the new CSC Coefficients at the next Vsync rising edge 0 = Update Complete 1 = Allow CSC Update	4.3.8

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
0x1A	R/W	[12:0]	***00100	A2 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x1B			10101000			
0x1C	R/W	[12:0]	***00000	A3 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x1D			00000000			
0x1E	R/W	[12:0]	***11100	A4 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x1F			10000100			
0x20	R/W	[12:0]	***11100	B1 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x21			10111111			
0x22	R/W	[12:0]	***00100	B2 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x23			10101000			
0x24	R/W	[12:0]	***11110	B3 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x25			01110000			
0x26	R/W	[12:0]	***00010	B4 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x27			00011110			
0x28	R/W	[12:0]	***00000	C1 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x29			00000000			
0x2A	R/W	[12:0]	***00100	C2 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x2B			10101000			
0x2C	R/W	[12:0]	***01000	C3 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x2D			00010010			
0x2E	R/W	[12:0]	***11011	C4 (CSC)	See description for registers 0x18 and 0x19	4.3.8
0x2F			10101100			
0x30	R/W	[9:0]	00000000	Hsync Placement (Embedded Sync Decoder)	Upper 8 bits for Embedded Sync Decoder Hsync Placement (In Pixels)	4.3.7
0x31			00******			
0x31	R/W	[9:0]	**000000	Hsync Duration (Embedded Sync Decoder)	Upper 6 bit for Embedded Sync Decoder Hsync Duration (In Pixels)	4.3.7
0x32			0000****			
0x32	R/W	[9:0]	****0000	Vsync Placement (Embedded Sync Decoder)	Upper 4 bits for Embedded Sync Decoder Vsync Placement (In Hsyncs)	4.3.7
0x33			000000**			
0x33	R/W	[9:0]	******00	Vsync Duration (Embedded Sync Decoder)	Upper 2 bit for Embedded Sync Decoder Vsync Duration (In Hsyncs)	4.3.7
0x34			00000000			
0x35	R/W	[9:0]	00000000	Hsync Delay (DE Generator)	Upper 8 bits for DE Generation Hsync Delay (In Pixels)	4.3.7
0x36			00******			
0x36	R/W	[5:0]	**000000	Vsync Delay (DE Generator)	Vsync Delay for DE Generation. (In Hsyncs)	4.3.7

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
0x37	R/W	[7:5]	000*****	Interlace Offset (DE Generator)	Interlace Offset For DE Generation Sets the difference (in hsyncs) in field length between field 0 and field 1	4.3.7
0x37	R/W	[11:0]	***00000	Active Width (DE Generator)	Upper 5 bits for DE Generation Active Width (In Pixels)	4.3.7
0x38			0000000*			
0x39	R/W	[11:0]	00000000	Active Height (DE Generator)	Upper 8 bits for DE Generation Active Height (In Lines)	4.3.7
0x3A			0000****			
0x3B	R/W	[7]	1*******	Reserved @ 1b	Must be set to Default Value	
		[6:5]	*00*****	PR Mode	Pixel Repetition Mode Selection. Set to b00 unless non-standard video is supported. 00 = auto mode 01 = max mode 10 = manual mode 11 = manual mode	4.3.4
		[4:3]	***00***	PR PLL Manual	The clock multiplication of the input clock used in pixel repetition. 00 = x1 01 = x2 10 = x4 11 = x4	4.3.4
		[2:1]	*****00*	PR Value Manual	User programmed pixel repetition number to send to Rx. 00 = x1 01 = x2 10 = x4 11 = x4	4.3.4
		[0]	*******0	Reserved @ 0b	Must be set to Default Value	
0x3C	R/W	[5:0]	**000000	VIC Manual	User programmed VIC to sent to Rx (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9	4.3.4

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use	
0x3D	RO	[7:6]	00******	Pixel Repeat to Rx	The actual pixel repetition sent to Rx 00 = x1 01 = x2 10 = x4 11 = x4	4.3.4
		[5:0]	**000000	VIC to Rx	VIC sent to HDMI Rx and Used in the AVI InfoFrame Status (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9	4.3.3 4.3.4

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9 110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9	

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use	
0x3E	RO	[7:2]	000000**	VIC Detected	Input VIC Detected (value defined in CEA861D) 000000 = VIC#0: VIC Unavailable 000001 = VIC#1: VGA (640x480) 4:3 000010 = VIC#2: 480p-60, 4:3 000011 = VIC#3: 480p-60, 16:9 000100 = VIC#4: 720p-60, 16:9 000101 = VIC#5: 1080i-60, 16:9 000110 = VIC#6: 480i-60, 2x Clk, 4:3 000111 = VIC#7: 480i-60, 2x Clk, 16:9 001000 = VIC#8: 240p-60, 2x Clk, 4:3 001001 = VIC#9: 240p-60, 2x Clk, 16:9 001010 = VIC#10: 480i-60, 4x Clk, 4:3 001011 = VIC#11: 480i-60, 4x Clk, 16:9 001100 = VIC#12: 240p-60, 8x Clk, 4:3 001101 = VIC#13: 240p-60, 8x Clk, 16:9 001110 = VIC#14: 480p-60, 2x Clk, 4:3 001111 = VIC#15: 480p-60, 2x Clk, 16:9 010000 = VIC#16: 1080p-60, 16:9 010001 = VIC#17: 576p-50, 4:3 010010 = VIC#18: 576p-50, 16:9 010011 = VIC#19: 720p-50, 16:9 010100 = VIC#20: 1080i-50, 16:9 010101 = VIC#21: 576i-50, 2x Clk, 4:3 010110 = VIC#22: 576i-50, 2x Clk, 16:9 010111 = VIC#23: 288p-50, 2x Clk, 4:3 011000 = VIC#24: 288p-50, 2x Clk, 16:9 011001 = VIC#25: 576i-50, 4x Clk, 4:3 011010 = VIC#26: 576i-50, 4x Clk, 16:9 011011 = VIC#27: 288p-50, 8x Clk, 4:3 011100 = VIC#28: 288p-50, 8x Clk, 16:9 011101 = VIC#29: 576p-50, 2x Clk, 4:3 011110 = VIC#30: 576p-50, 2x Clk, 16:9 011111 = VIC#31: 1080p-50, 16:9 100000 = VIC#32: 1080p-24, 16:9 100001 = VIC#33: 1080p-25, 16:9 100010 = VIC#34: 1080p-30, 16:9 100011 = VIC#35: 480p-60, 4x Clk, 4:3 100100 = VIC#36: 480p-60, 4x Clk, 16:9 100101 = VIC#37: 576p-50, 4x Clk, 4:3 100110 = VIC#38: 576p-50, 4x Clk, 16:9 100111 = VIC#39: 1080i-50, Alt Blanking 101000 = VIC#40: 1080i-100, 16:9 101001 = VIC#41: 720p-100, 16:9 101010 = VIC#42: 576p-100, 4:3 101011 = VIC#43: 576p-100, 16:9 101100 = VIC#44: 576i-100, 4:3 101101 = VIC#45: 576i-100, 16:9 101110 = VIC#46: 1080i-120, 16:9 101111 = VIC#47: 720p-120, 16:9 110000 = VIC#48: 480p-120, 4:3 110001 = VIC#49: 480p-120, 16:9	4.3.3

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					110010 = VIC#50: 480i-120, 4:3 110011 = VIC#51: 480i-120, 16:9 110100 = VIC#52: 576p-200, 4:3 110101 = VIC#53: 576p-200, 16:9 110110 = VIC#54: 576i-200, 4:3 110111 = VIC#55: 576i-200, 16:9 111000 = VIC#56: 480p-240, 4:3 111001 = VIC#57: 480p-240, 16:9 111010 = VIC#58: 480i-240, 4:3 111011 = VIC#59: 480i-240, 16:9 111100 = VIC#60: 60+ For Future Use	
0x3F	RO	[7:5]	000*****	Auxiliary VIC Detected	This register is for video input formats that are not inside the 861D table. 000 = Set by Register 0x3E 001 = 240p Not Active 010 = 576i not active 011 = 288p not active 100 = 480i active 101 = 240p active 110 = 576i active 111 = 288p active	4.3.3
		[4:3]	***00***	Progressive Mode Information	Information about 240p and 288p modes. Case 1: 240p 01 = 262 lines 10 = 263 lines Case 2: 288p 01 = 312 lines 10 = 313 lines 11 = 314 lines	4.3.3
0x40	R/W	[7]	0*******	GC Packet Enable	GC Packet Enable 0 = GC Packet Disabled 1 = GC Packet Enabled	4.2.3 4.3.3
		[6]	*0******	SPD Packet Enabled	SPD Packet Enable 0 = Disabled 1 = Enabled	4.2.5
		[5]	**0*****	MPEG Packet Enabled	MPEG Packet Enable 0 = Disabled 1 = enable	4.3.9.2
		[4]	***0****	ACP Packet Enable	ACP Packet Enable 0 = Disabled 1 = Enabled	4.4.5
		[3]	****0***	ISRC Packet Enable	ISRC Packet Enable 0 = Disabled 1 = Enabled	
		[2]	*****0**	GM Packet Enable	GM Packet Enable 0 = Disabled 1 = Enabled	4.3.9.3
		[1]	******0*	Spare Packet 2 Enable	Spare Packet 2 Enable 0 = Disabled	4.2.7

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					1 = Enabled	
		[0]	*******0	Spare Packet 1 Enable	Spare Packet 1 Enable 0 = Disabled 1 = Enabled	4.2.7
0x41	R/W	[6]	*1******	POWER DOWN	Main Power Down 0 = all circuits powered up 1 = power down whole chip, except I2C,HPD interrupt,Monitor Sense interrupt,CEC 0 = Normal Operation 1 = ADV7511 Powered Down	4.8.1
		[5]	**0*****	Fixed	Must be set to Default Value	
		[4]	***1****	Reserved @ 1b	Must be set to Default Value	
		[3:2]	****00**	Fixed	Must be set to Default Value	
		[1]	******0*	Sync Adjustment Enable	Enable Sync Adjustment 0 = Disabled 1 = Enabled	4.3.3
		[0]	*******0	Fixed	Must be set to Default Value	
0x42	RO	[7]	1*******	Power Down Polarity	Polarity for chip pin , Default is 1 0 = active low 1 = active high	4.8.1
		[6]	*0******	HPD State	State of HDMI sink 0 = Hot Plug Detect state is low 1 = Hot Plug Detect state is high	4.2.1
		[5]	**0*****	Monitor Sense State	state of the monitor connection 0 = HDMI clock termination not detected 1 = HDMI clock termination detected	4.2.1
		[4]	***1****	Fixed		
		[3]	****0***	I2S 32 Bit Mode Detect	I2S Mode Detections Shows the number of SCLK periods per LRCLK period. 0 = 32 bit mode detected 1 = 64 bit mode detected	4.4.1
		[2]	*****0**	Fixed		
0x43	R/W	[7:0]	01111110	EDID Memory Address	The I2C address for EDID memory	4.1
0x44	R/W	[7]	0*******	Reserved @ 0b	Must be set to Default Value	
		[6]	*1******	N CTS Packet Enable	N CTS Packet Enable 0 = Disabled 1 = Enabled	4.4.2
		[5]	**1*****	Audio Sample Packet Enable	Audio Sample Packet Enable 0 = Disabled 1 = Enabled	4.4.3
		[4]	***1****	AVI InfoFrame Enable	AVI InfoFrame Enable 0 = Disabled	4.3.9.1

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					1 = Enabled	
		[3]	****1***	Audio InfoFrame Enable	Audio InfoFrame Enable 0 = Disabled 1 = Enabled	4.4.4
		[2:1]	*****00*	Fixed	Must be set to Default Value	
		[0]	*******1	Packet Read Mode	Packet Memory Read Mode 0=Allow user to read from packet memory 1=Allow HDMI logic to read from packet memory	4.1
0x45	R/W	[7:0]	01110000	Packet Memory I2C Map Address	I2C address for the packet memory	4.1
0x46	R/W	[7:0]	00000000	DSD Enable	DSD Channel Enable Each bit enables one of the 8 DSD audio input channels. Bit 0 enables channel 0, and bit 7 enables channel 7.	4.4.1.3
0x47	R/W	[7]	0*******	DSD Mux Enable	DSD Mux Enable. User has to set this bit to one to use DSD[7:6]. 0 = Disabled 1 = Enabled	4.4.1.3
		[6]	*0******	PaPb Sync	For HBR audio this syncs PaPb with sub packet 0.	4.4.1.4
		[5]	**0*****	Audio Sample 3 Valid	Indicates when sub packet 3 has invalid data.	4.4.3
		[4]	***0****	Audio Sample 2 Valid	Indicates when sub packet 2 has invalid data.	
		[3]	****0***	Audio Sample 1 Valid	Indicates when sub packet 1 has invalid data.	
		[2]	*****0**	Audio Sample 0 Valid	Indicates when sub packet 0 has invalid data.	
0x48	R/W	[7]	0*******	Reserved	Must be set to Default Value	
		[6]	*0******	Video Input Bus Reverse	Bit order reverse for input signals. 0 = Normal Bus Order 1 = LSB .... MSB Reverse Bus Order	4.3.1
		[5]	**0*****	DDR Alignment	DDR alignment (Only For ID 5) See ►Table 23 - ►Table 27 0 = DDR input is D[17:0] 1 = DDR input is D[35:18]	4.3.1
		[4:3]	***00***	Video Input Justification	Bit Justfication for YCbCr 4:2:2 modes. See ►Table 17 to ►Table 22 and ►Table 25 to ►Table 27 00 = evenly distributed 01 = right justified 10 = left justified 11 = Invalid	4.3.1
0x49	R/W	[7:2]	101010**	Bit Trimming Mode	Bit Trimming Mode All other settings are invalid 000000 = Active Dither	4.3.6

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					101010 = Truncate	
0x4A	R/W	[7]	1*******	Auto Checksum Enable	Auto Checksum Enable 0 = Use checksum from registers 1 = Use automatically generated checksum	0 4.3.9.1 4.3.9.2 4.4.4
		[6]	*0******	AVI Packet Update	AVI Packet Update: Before updating the AVI Packet using I2C set to '1' to continue sending the current values. 0 = AVI Packet I2C update inactive 1 = AVI Packet I2C update active	4.3.9.1
		[5]	**0*****	Audio InfoFrame Packet Update	Audio InfoFrame Packet Update: Before updating the Audio InfoFrame Packet using I2C set to '1' to continue sending the current values. 0 = Audio InfoFrame Packet I2C update inactive 1 = Audio InfoFrame Packet I2C update active	4.4.4
		[4]	***0****	GC Packet Update	GC Packet Update: Before updating the GC Packet using I2C set to '1' to continue sending the current values. 0 = GC Packet I2C update inactive 1 = GC Packet I2C update active	4.2.3 4.3.6
0x4B	R/W	[7]	0*******	Clear AV Mute	Clear Audio Video Mute 0 = Clear 1 = Set clear av mute	4.2.3
		[6]	*0******	Set AV Mute	Set Audio Video Mute 0 = Clear 1 = Set av mute.	4.2.3
0x4C	RO	[7:4]	0000****	Pixel Packing (GC Packet)	Pixel packing phase for Deep Color conversion. (Read Only)	4.3.6
		[3:0]	****0000	Color Depth (GC Packet)	Color depth of video to Rx All other settings are invalid 0000 = Color Depth Not Indicated 0100 = 24 Bits/Pixel 0101 = 30 Bits/Pixel 0110 = 36 Bits/Pixel	4.3.6
0x4D	R/W	[7:0]	00000000	GC Byte 2	Reserved in CEA 861D	
0x4E	R/W	[7:0]	00000000	GC Byte 3	Reserved in CEA 861D	
0x4F	R/W	[7:0]	00000000	GC Byte 4	Reserved in CEA 861D	
0x50	R/W	[7:0]	00000000	GC Byte 5	Reserved in CEA 861D	
0x51	R/W	[7:0]	00000000	GC Byte 6	Reserved in CEA 861D	
0x52	R/W	[2:0]	*****010	AVI InfoFrame Version	Version of AVI InfoFrame Should be left default	4.3.9.1
0x53	R/W	[4:0]	***01101	AVI InfoFrame Length	Length of packet body, excluding checksum	4.3.9.1
0x54	R/W	[7:0]	00000000	AVI InfoFrame Checksum	Checksum for AVI IF. Only used in manual checksum mode..	4.3.9.1
0x55	R/W	[7]	0*******	AVI Byte 1 bit 7	Reserved per HDMI spec. - set to 0	4.3.9.1

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
		[6:5]	*00*****	Y1Y0 (AVI InfoFrame)	Output format - this should be written when 0x16[7:6] is written. 00 = RGB 01 = YCbCr 4:2:2 10 = YCbCr 4:4:4 11 = reserved	4.3.9.1
		[4]	***0****	Active Format Information Status (AVI InfoFrame)	Active Format Information Present 0 = no data 1 = Active format Information valid	4.3.9.1
		[3:2]	****00**	Bar Information (AVI InfoFrame)	B[1:0] 00 = invalid bar 01 = vertical 10 = horizontal 11 = Both	4.3.9.1
		[1:0]	******00	Scan Information (AVI InfoFrame)	S[1:0] 00 = no data 01 = TV 10 = PC 11 = None	4.3.9.1
0x56	R/W	[7:6]	00******	Colorimetry (AVI InfoFrame)	C[1:0] 00 = no data 01 = ITU601 10 = ITU709 11 = Extended Colorimetry Information Valid (Indicated in register 0x57[6:4])	4.3.9.1
		[5:4]	**00****	Picture Aspect Ratio (AVI InfoFrame)	M[1:0] 00 = no data 01 = 4:3 10 = 16:9 11 = None	4.3.9.1
		[3:0]	****0000	Active Format Aspect Ratio (AVI InfoFrame)	R[3:0] 1000 = Same as Aspect Ratio 1001 = 4:3 (center) 1010 = 16:9 (center) 1011 = 14:9 (center)	4.3.9.1
0x57	R/W	[7]	0*******	ITC	IT Content 0 = None 1 = IT content available in register bits 0x59[5:4]	4.3.9.1
		[6:4]	*000****	EC[2:0]	E[2:0] All other values reserved per HDMI 1.4 Specification 000 = xvYCC 601 001 =xvYCC 709 010 = sYCC601 011 = AdobeYCC601 100 = AdobeRGB	4.3.9.1
		[3:2]	****00**	Q[1:0]	RGB Quantization range 00 = default range 01 = limited range 10 = full range	4.3.9.1

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					11 = reserved	
		[1:0]	******00	Non-Uniform Picture Scaling (AVI InfoFrame)	SC[1:0] 00 = unknown 01 = scaling in Horizontal direction 10 = scaling in Vertical direction 11 = scaling in Both H & V directions	4.3.9.1
0x58	R/W	[7]	0*******	Byte 4 Bit 7 (AVI InfoFrame)	Reserved per HDMI spec. Set to '0'.	4.3.9.1
0x59	R/W	[7:4]	0000****	Byte 5 bit [7:4] (AVI InfoFrame)	YQ[1:0] 00 = Limited Range 01 = Full Range 10 = Reserved 11 = Reserved	4.3.9.1
0x5A	R/W	[7:0]	00000000	Active Line Start LSB (AVI InfoFrame)	Active Line Start This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.	4.3.9.1
0x5B	R/W	[7:0]	00000000	Active Line Start MSB (AVI InfoFrame)	Active Line Start This represents the line number of the end of the top horizontal bar. If 0, there is no horizontal bar.	4.3.9.1
0x5C	R/W	[7:0]	00000000	Active Line End LSB (AVI InfoFrame)	Active Line End This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.	4.3.9.1
0x5D	R/W	[7:0]	00000000	Active Line End MSB (AVI InfoFrame)	Active Line End This represents the line number of the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.	4.3.9.1
0x5E	R/W	[7:0]	00000000	Active Pixel Start LSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.	4.3.9.1
0x5F	R/W	[7:0]	00000000	Active Pixel Start MSB (AVI InfoFrame)	Active Pixel Start This represents the last pixel in a vertical pillar-bar at the left side of the picture. If 0, there is no left bar.	4.3.9.1
0x60	R/W	[7:0]	00000000	Active Pixel End LSB (AVI InfoFrame)	Active Pixel End This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.	4.3.9.1
0x61	R/W	[7:0]	00000000	Active Pixel End MSB (AVI InfoFrame)	Active Pixel End This represents the first horizontal pixel in a vertical pillar-bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.	4.3.9.1
0x62	R/W	[7:0]	00000000	Byte 14 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x63	R/W	[7:0]	00000000	Byte 15 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x64	R/W	[7:0]	00000000	Byte 16 (AVI	Reserved per HDMI spec. Set to 0x00.	4.3.9.1

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
				InfoFrame)		
0x65	R/W	[7:0]	00000000	Byte 17 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x66	R/W	[7:0]	00000000	Byte 18 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x67	R/W	[7:0]	00000000	Byte 19 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x68	R/W	[7:0]	00000000	Byte 20 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x69	R/W	[7:0]	00000000	Byte 21 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x6A	R/W	[7:0]	00000000	Byte 22 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x6B	R/W	[7:0]	00000000	Byte 23 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x6C	R/W	[7:0]	00000000	Byte 24 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x6D	R/W	[7:0]	00000000	Byte 25 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x6E	R/W	[7:0]	00000000	Byte 26 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x6F	R/W	[7:0]	00000000	Byte 27 (AVI InfoFrame)	Reserved per HDMI spec. Set to 0x00.	4.3.9.1
0x70	R/W	[2:0]	*****001	Audio InfoFrame Version	Version of Audio InfoFrame Set to 001 as defined in CEA861	
0x71	R/W	[4:0]	***01010	Audio InfoFrame Length	Length of packet body, excluding checksum	
0x72	R/W	[7:0]	00000000	Audio InfoFrame Checksum	Checksum for AVI InfoFrame packet. Only used in manual checksum mode.	
0x73	R/W	[7:4]	0000****	Coding Type (Audio InfoFrame)	Coding Type Set to 0 according to HDMI Specification 1.4	
		[3]	****0***	Byte 1 bit 3 (Audio InfoFrame)	Fixed per HDMI spec. Set to 0.	
		[2:0]	*****000	CC (Audio InfoFrame)	Channel Count 000 = Refer to Stream Header 001 = 2 channels 010 = 3 channels 011 = 4 channels 100 = 5 channels 101 = 6 channels 110 = 7 channels 111 = 8 channels	
0x74	R/W	[7:5]	000*****	Byte 2 bit [7:5] (Audio InfoFrame)	Fixed per HDMI spec. Set to 0.	4.4.4

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
		[4:2]	***000**	Sampling Frequency (Audio InfoFrame)	Audio sampling frequency. Should be 0, except for SACD.	4.4.4
		[1:0]	******00	Sample Size (Audio InfoFrame)	Set to 0	4.4.4
0x75	R/W	[7:0]	00000000	Byte 3 (Audio InfoFrame)	Set to 0	4.4.4
0x76	R/W	[7:0]	00000000	Speaker Mapping (Audio InfoFrame)	CA[7:0] Speaker mapping or placement for up to 2 channels.	4.4.4
0x77	R/W	[7]	0*******	DM_INH (Audio InfoFrame)	Down-mix Inhibit	4.4.4
		[6:3]	*0000***	Level Shift (Audio InfoFrame)	LSV[3:0]-Audio Level Shift Values With Attenuation Information 0000 = 0dB attenuation 0001 = 1dB attenuation 0010 = 2dB attenuation 0011 = 3dB attenuation 0100 = 4dB attenuation 0101 = 5dB attenuation 0110 = 6dB attenuation 0111 = 7dB attenuation 1000 = 8dB attenuation 1001 = 9dB attenuation 1010 = 10dB attenuation 1011 = 11dB attenuation 1100 = 12dB attenuation 1101 = 13dB attenuation 1110 = 14dB attenuation 1111 = 15dB attenuation	4.4.4
		[2]	*****0**	Byte 5 bit [2]	Fixed per HDMI spec	4.4.4
		[1:0]	******00	LFEPBL[1:0]	Set to 0b0,ow Frequency Effect Playback Level 00 = No information 01 = 0 dB playback 10 = +10 dB playback 11 = Reserved	4.4.4
0x78	R/W	[7:0]	00000000	Byte 6 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'	4.4.4
0x79	R/W	[7:0]	00000000	Byte 7 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'	4.4.4
0x7A	R/W	[7:0]	00000000	Byte 8 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'	4.4.4
0x7B	R/W	[7:0]	00000000	Byte 9 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'	4.4.4
0x7C	R/W	[7:0]	00000000	Byte 10 (Audio InfoFrame)	Reserved per HDMI spec. Set to '0x00'	4.4.4
0x92	R/W	[7]	0*******	Wake Up Opcode8Interrupt	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode8in CEC message	4.9.5 4.10

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
				Enable	0 = Interrupt Disabled 1 = Interrupt Enabled	
		[6]	*0******	Wake Up Opcode7Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode7in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled	4.9.5 4.10
		[5]	**0*****	Wake Up Opcode6Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode6in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled	4.9.5 4.10
		[4]	***0****	Wake Up Opcode5Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode5in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled	4.9.5 4.10
		[3]	****0***	Wake Up Opcode4Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode4in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled	4.9.5 4.10
		[2]	*****0**	Wake Up Opcode3Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode3in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled	4.9.5 4.10
		[1]	******0*	Wake Up Opcode2Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode2in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled	4.9.5 4.10
		[0]	*******0	Wake Up Opcode1Interrupt Enable	CEC Wake Up Code Interrupt Enable Enable interrupt detecting Wake Up Opcode1in CEC message 0 = Interrupt Disabled 1 = Interrupt Enabled	4.9.5 4.10
0x93	R/W	[7]	0*******	Wake Up Opcode8Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode8in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5
		[6]	*0******	Wake Up Opcode7Interrupt	CEC Wake Up Code Interrupt Enable interrupt detecting Wake Up Opcode7in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5 4.10

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
		[5]	**0*****	Wake Up Opcode6Interrupt	CEC Wake Up Code Interrupt Enable Interrupt detecting Wake Up Opcode6in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5 4.10
		[4]	***0****	Wake Up Opcode5Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode5in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5 4.10
		[3]	****0***	Wake Up Opcode4Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode4in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5 4.10
		[2]	*****0**	Wake Up Opcode3Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode3in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5 4.10
		[1]	******0*	Wake Up Opcode2Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode2in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5 4.10
		[0]	*******0	Wake Up Opcode1Interrupt	CEC Wake Up Code Interrupt Interrupt detecting Wake Up Opcode1in CEC message 0= No Interrupt Detected 1 = Interrupt Detected	4.9.5 4.10
0x94	R/W	[7]	1*******	HPD Interrupt Enable	HPD Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.2.1 4.10
		[6]	*1******	Monitor Sense Interrupt Enable	Monitor Sense Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.2.1
		[5]	**0*****	Vsync Interrupt Enable	Vsync Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.10
		[4]	***0****	Audio FIFO Full Interrupt Enable	Audio FIFO Full Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.4.1 4.10
		[3]	****0***	Fixed	Must be set to Default Value	
		[2]	*****0**	EDID Ready Interrupt Enable	EDID Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.6 4.10
		[1]	******0*	HDCP	HDCP Authenticated Interrupt Enable	4.7

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
				Authenticated Interrupt Enable	0 = interrupt disabled 1 = interrupt enabled	4.10
		[0]	*******0	Fixed	Must be set to Default Value	
0x95	R/W	[7]	0*******	DDC Controller Error Interrupt Enable	DDC Controller Error Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.2.8 4.10
		[6]	*0******	BKSV Flag Interrupt Enable	BKSV Flag Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.7 4.10
		[5]	**0*****	Tx Ready Interrupt Enable	CEC Tx Ready Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.9.2 4.10
		[4]	***0****	Tx Arbitration Lost Interrupt Enable	CEC Tx Arbitration Lost Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.9.2 4.10
		[3]	****0***	Tx Retry Timeout Interrupt Enable	CEC Tx Retry Timeout Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.9.2 4.10
		[2]	*****0**	Rx Ready 3 Interrupt Enable	CEC Rx Ready 3 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.9.3 4.10
		[1]	******0*	Rx Ready 2 Interrupt Enable	CEC Rx Ready 2 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.9.3 4.10
		[0]	*******0	Rx Ready 1 Interrupt Enable	CEC Rx Ready 1 Interrupt Enable 0 = interrupt disabled 1 = interrupt enabled	4.9.3 4.10
0x96	R/W	[7]	0*******	HPD Interrupt	HPD Interrupt 0 = no interrupt detected 1 = interrupt detected	4.2.1 4.10
		[6]	*0******	Monitor Sense Interrupt	Monitor Sense Interrupt 0 = no interrupt detected 1 = interrupt detected	4.2.1
		[5]	**0*****	Vsync Interrupt	Vsync Interrupt 0 = no interrupt detected 1 = interrupt detected	4.10
		[4]	***0****	Audio FIFO Full Interrupt	Audio FIFO Full Interrupt 0 = no interrupt detected 1 = interrupt detected	4.4.1 4.10
		[3]	****0***	Fixed	Must be set to Default Value	
		[2]	*****0**	EDID Ready Interrupt	EDID Ready Interrupt 0 = no interrupt detected 1 = interrupt detected	4.6 4.10
		[1]	******0*	HDCP Authenticated	HDCP Authenticated 0 = no interrupt detected	4.7 4.10

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					1 = interrupt detected	
		[0]	*******0	Fixed @ 0b	Reserved	4.10
0x97	R/W	[7]	0*******	DDC Controller Error Interrupt	DDC Controller Error Interrupt 0 = no interrupt detected 1 = interrupt detected	4.2.8 4.10
		[6]	*0******	BKSV Flag Interrupt	BKSV Flag Interrupt 0 = no interrupt detected 1 = interrupt detected	4.7 4.10
		[5]	**0*****	Tx Ready Interrupt	CEC Tx Ready Interrupt 0 = no interrupt detected 1 = interrupt detected	4.9.2 4.10
		[4]	***0****	Tx Arbitration Lost Interrupt	CEC Tx Arbitration Lost interrupt 0 = no interrupt detected 1 = interrupt detected	4.9.2 4.10
		[3]	****0***	Tx Retry Timeout Interrupt	CEC Tx Retry Timeout interrupt 0 = no interrupt detected 1 = interrupt detected	4.9.2 4.10
		[2]	*****0**	Rx Ready 3 Interrupt	CEC Rx Ready 3 Interrupt 1 = interrupt detected for rx buffer 3 0 = no interrupt detected for buffer 3 1 = interrupt detected for buffer 3 0 = no interrupt detected for buffer 3	4.9.2 4.10
		[1]	******0*	Rx Ready 2 Interrupt	CEC Rx Ready 2 Interrupt 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2 1 = interrupt detected for buffer 2 0 = no interrupt detected for buffer 2	4.9.2 4.10
		[0]	*******0	Rx Ready 1 Interrupt	CEC Rx Ready 1 Interrupt 1 = interrupt detected for rx buffer 1 0 = no interrupt detected for buffer 1 1 = interrupt detected for buffer 1 0 = no interrupt detected for buffer 1	4.9.2 4.10
0x98	R/W	[7:0]	00001011	Fixed	Must be set to 0x03 for proper operation.	
0x99	R/W	[7:0]	00000010	Fixed	Must be set to Default Value	
0x9A	R/W	[7:1]	0000000*	Fixed	Must be set to 0b1110000 for proper operation	
0x9B	R/W	[5:0]	**011000	Fixed	Must be set to Default Value	
0x9C	R/W	[7:0]	01011010	Fixed	Must be set to 0x30 for proper operation	
0x9D	R/W	[7:4]	0110****	Fixed	Must be set to Default Value	
		[3:2]	****00**	Input Pixel Clock Divide	Input Video CLK Divide 00 = Input Clock not Divided 01 = Input Clock Divided by 2 10 = Input Clock Divided by 4 11 = Invalid Setting	
		[1:0]	******00	Fixed	Must be set to 0b01 for proper operation.	

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
0x9E	RO	[4]	***0****	PLL Lock Status	PLL Lock Status 0 = PLL Not Locked 1 = PLL Locked	4.2.8
		[3:0]	****0000	Fixed		
0x9F	R/W	[7:0]	00000000	Fixed	Must be set to Default Value	
0xA0	RO	[7:0]	00000000	Fixed		
0xA1	R/W	[7]	0*******	Fixed	Must be set to Default Value	
		[6]	*0******	Monitor Sense Power Down	Monitor Sense Power Down 0 = Monitor Sense monitoring enabled 1 = Monitor Sense monitoring disabled	4.2.1 4.8.1 4.10
		[5]	**0*****	Channel 0 Power Down	Channel 0 Power Down 0 = power up 1 = power down	4.2.4
		[4]	***0****	Channel 1 Power Down	Channel 1 Power Down 0 = power up 1 = power down	4.2.4
		[3]	****0***	Channel 2 Power Down	Channel 2 Power Down 0 = power up 1 = power down	4.2.4
		[2]	*****0**	Clock Driver Power Down	Clock Driver Power Down 0 = power up 1 = power down	4.2.4
0xA2	R/W	[7:0]	10000000	Fixed	Must be set to 0xA4 for proper operation	
0xA3	R/W	[7:0]	10000000	Fixed	Must be set to 0xA4 for proper operation	
0xA4	R/W	[7:1]	0000100*	Fixed	Must be set to Default Value	
0xA5	R/W	[7:1]	0000010*	Fixed	Must be set to Default Value	
0xA6	R/W	[7:0]	00000000	Fixed	Must be set to Default Value	
0xA7	R/W	[7:0]	00000000	Fixed	Must be set to Default Value	
0xA8	R/W	[7:0]	00000000	Fixed	Must be set to Default Value	
0xA9	R/W	[7:1]	0000000*	Fixed	Must be set to Default Value	
0xAA	R/W	[7:0]	00000000	Fixed	Must be set to Default Value	
0xAB	R/W	[7:3]	01000***	Fixed	Must be set to Default Value	
0xAC	RO	[7:0]	00000000	Fixed		
0xAD	RO	[7:0]	00000000	Fixed		
0xAE	RO	[7:5]	010*****	Fixed		
0xAF	R/W	[7]	0*******	HDCP Enable	Enable HDCP 0 = HDCP Disabled 1 = HDCP Encryption Enabled	4.7
		[6:5]	*00*****	Fixed	Must be set to Default Value	
		[4]	***1****	Frame Encryption	Enable HDCP Frame Encryption	4.7

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					0 = Current Frame NOT HDCP Encrypted 1 = Current Frame HDCP Encrypted	
		[3:2]	****01**	Fixed	Must be set to Default Value	
		[1]	******0*	HDMI/DVI Mode Select	HDMI Mode 0 = DVI Mode 1 = HDMI Mode	4.2.2
		[0]	*******0	Fixed	Must be set to Default Value	
0xB0	RO	[7:0]	00000000	Byte 0 of An or AKSV Byte 0	Byte 0 of An or AKSV Byte 0	4.7
0xB1	RO	[7:0]	00000000	Byte 1 of An or AKSV Byte 1	Byte 1 of An or AKSV Byte 1	4.7
0xB2	RO	[7:0]	00000000	Byte 2 of An or AKSV Byte 2	Byte 2 of An or AKSV Byte 2	4.7
0xB3	RO	[7:0]	00000000	Byte 3 of An or AKSV Byte 3	Byte 3 of An or AKSV Byte 3	4.7
0xB4	RO	[7:0]	00000000	Byte 4 of An or AKSV Byte 4	Byte 4 of An or AKSV Byte 4	4.7
0xB5	RO	[7:0]	00000000	Byte 5 of An	byte 5 of An	4.7
0xB6	RO	[7:0]	00000000	Byte 6 of An	byte 6 of An	4.7
0xB7	RO	[7:0]	00000000	Byte 7 of An	byte 7 of An	4.7
0xB8	RO	[7]	0*******	Fixed		
		[6]	*0******	HDCP Encryption Status	1 means the A/V content is being encrypted at present. 0 = A/V Not Encrypted 1 = A/V Encrypted	4.7
		[5]	**0*****	Fixed		
		[4]	***0****	Key Read Error	1 means HDCP key reading error. 0 = Read HDCP Keys Correctly 1 = Errors Encountered Reading HDCP Keys	4.7
0xB9	R/W	[7:0]	00000000	Fixed	Must be set to Default Value	
0xBA	R/W	[7:5]	000*****	Clock Delay	Programmable delay for input video clock. Default is 0 for no delay. 000 = -1.2ns 001 = -0.8ns 010 = -0.4ns 011 = no delay 100 = 0.4ns 101 = 0.8ns 110 = 1.2ns 111 = 1.6ns	4.3.1
		[4]	***1****	Internal/External HDCP EEPROM	1 means internal EEPROM is used. This would turn on the on-chip pullup resistor for MCL and MDA. 0 = external EEPROM 1 = internal EEPROM	

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
		[3]	****0***	Fixed	Must be set to Default Value	
		[2]	*****0**	Display AKSV	Show AKSV in registers 0xB0 to 0xB4, Check Ri' before and after update, Must be set to Default 0 = Don't Show AKSV 1 = Show AKSV in 0xB0 - 0xB4	4.7
		[1]	******0*	Ri Two Point Check	Ri Two Point Check. Check Ri' before and after update. 0 = HDCP Ri standard 1 = enable HDCP Ri two point check	4.7
0xBB	R/W	[7:0]	00000000	Fixed	Must be set to Default Value	
0xBC	RO	[7:0]	00000000	Fixed		
0xBD	RO	[7:0]	00000000	Fixed		
0xBE	RO	[7:0]	00000000	BCAPS	HDCP related register [7] Reserved, [6] Repeater, [5] BKSV FIFO ready, [4] Fast DDC Bus, [3:2] Reserved, [1] HDCP 1.1 Features, [0] Fast Re-Authentication.	4.7
0xBF	RO	[7:0]	00000000	BKSV Byte 0	Bksv read from Rx by the DDC Controller	4.7
0xC0	RO	[7:0]	00000000	BKSV Byte 1	Bksv read from Rx by the DDC Controller	4.7
0xC1	RO	[7:0]	00000000	BKSV Byte 2	Bksv read from Rx by the DDC Controller	4.7
0xC2	RO	[7:0]	00000000	BKSV Byte 3	Bksv read from Rx by the DDC Controller	4.7
0xC3	RO	[7:0]	00000000	BKSV Byte 4	Bksv read from Rx by the DDC Controller	4.7
0xC4	R/W	[7:0]	00000000	EDID Segment	Sets the E-DDC segment used by the EDID Fetch routine.	4.6
0xC5	R/W	[7:0]	00000000	Fixed		
0xC6	RO	[7:0]	00000000	Fixed		
0xC7	R/W	[7]	0*******	Fixed	Must be set to Default Value	
	RO	[6:0]	*0000000	BKSV Count	BKSVs Available in Sink's BKSV FIFO	4.7
0xC8	RO	[7:4]	0000****	DDC Controller Error	DDC Controller Error Error code report when the DDC Controller Error Interrupt register 0x97[7] = 1	4.2.8 4.7
		[3:0]	****0000	DDC Controller State	DDC Controller State State of the controller used for HDCP debug purposes	4.2.8 4.7
0xC9	R/W	[4]	***0****	EDID Reread	Rereads current segment if toggled from 0 to 1 0 = disable 1 = enable	4.6
		[3:0]	****0011	EDID Tries	Maximum number of times that the EDID read will be attempted if unsuccessful.	4.6
0xCA	RO	[7:0]	00000000	HDCP BSTATUS[15:8]	BSTATUS information for HDCP [15:8]	4.7
0xCB	RO	[7:0]	00000000	HDCP BSTATUS[7:0]	BSTATUS information for HDCP [7:0]	4.7
0xCC	RO	[2:0]	*****000	Fixed		
0xCD	R/W	[7:4]	0000****	Fixed	Must be set to Default Value	

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
0xCE	R/W	[7:0]	00000001	Fixed	Must be set to Default Value	
0xCF	R/W	[7:0]	00000100	Fixed	Must be set to Default Value	
0xD0	R/W	[7]	0*******	Enable DDR Negative Edge CLK Delay	Enable DDR Negative Edge Clock Delay Adjust 0 = Disable DDR Negative Edge CLK Delay 1 = Enable DDR Negative Edge CLK Delay	4.3.1
		[6:4]	*011****	DDR Negative Edge CLK Delay	Delay Adjust for the Input Video CLK Negative Edge for DDR Capture Should be set to 0b011 for No Delay 000 = -1200 ps 001 = -800 ps 010 = -400 ps 011 = no delay 100 = 400 ps 101 = 800 ps 110 = 1200 ps 111 = Invert CLK	4.3.1
		[3:2]	****00**	Sync Pulse Select	Case 1: Input ID register bits (0x15[3:0] = 5,6,7,8 Must be 0b11 Case 2: For input ID 1, 2, 3, 4 with 1X clock (See the Input Data Clock section, number 0). Can be set to any value. Case 3: For 2X or 4X input clock (See Input Data Clock section) with ID 1, 2, 3, 4. 1X generated clock synchronizes with. 00 = DE 01 = Hsync 10 = Vsync 11 = no sync pulse	4.3.1
		[1]	******0*	Timing Generation Sequence	Timing Generation Sequence 0 = sync adjustment then DE generation 1 = DE generation then sync adjustment	4.3.7
		[0]	*******0	Fixed	Must be set to Default Value	
0xD1	R/W	[7:0]	11111111	Fixed	Must be set to Default Value	
0xD2	R/W	[7:0]	10000000	Fixed	Must be set to Default Value	
0xD3	R/W	[7:0]	10000000	Fixed	Must be set to Default Value	
0xD4	R/W	[7:0]	10000000	Fixed	Must be set to Default Value	
0xD5	R/W	[7:4]	0000****	Fixed	Must be set to Default Value	
		[3:2]	****00**	High Refresh Rate Video	High Refresh Rate Video for VIC Detection 00 = normal refresh rate 01 = 2x refresh rate 10 = 4x refresh rate 11 = not valid	4.3.3
		[1]	******0*	YCbCr Code Shift	YCbCr Code Shift 0 = Code Shift Disabled 1 = Code Shift Enabled	4.3.8
		[0]	*******0	Black Image	Black Image 0 = Black Image Disabled 1 = Black Image Enabled	4.3.8

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
0xD6	R/W	[7:6]	00******	HPD Control	HPD Control 00 = HPD is from both HPD pin or CDC HPD 01 = HPD is from CDC HPD 10 = HPD is from HPD pin 11 = HPD is always high	4.2.1
		[5]	**0*****	Fixed	Must be default for proper operation,	
		[4]	***0****	TMDS CLK Soft Turn On	Soft TMDS Clock Turn On 0 = Soft Turn On Disabled 1 = Soft Turn On Enabled	4.2.4
		[3:1]	****000*	Fixed	Must be set to Default Value	
		[0]	*******0	Audio and Video Input Gating	Audio and Video Input Gating 0 = video input and clock not gated 1 = video input and clock gated	4.8.2
0xD7	R/W	[9:0]	00000000	Hsync Placement (Sync Adjustment)	Hsync Front Porch (In Pixels)	4.3.7
0xD8			00******			
0xD8	R/W	[9:0]	**000000	Hsync Duration (Sync Adjustment)	Hsync Duration (In Pixels)	4.3.7
0xD9			0000****			
0xD9	R/W	[9:0]	****0000	Vsync Placement (Sync Adjustment)	Vsync Front Porch (In Hsyncs)	4.3.7
0xDA			000000**			
0xDA	R/W	[9:0]	******00	Vsync Duration (Sync Adjustment)	Vsync Duration (In Hsyncs)	4.3.7
0xDB			00000000			
0xDC	R/W	[7:5]	000*****	Offset (Sync Adjustment)	Offset for Sync Adjustment Vsync Placement Used only with interlaced formats (In Hsyncs)	4.3.7
0xDC	R/W	[8:0]	***00000	Fixed	Must be default for proper operation.	
0xDD			0000****			
0xDE	R/W	[7:4]	0001****	Fixed	Must be set to Default for proper operation.	
		[3]	****0***	TMDS Clock Inversion	TMDS Clock Inversion 0 = Normal TMDS Clock 1 = Inverted TMDS Clock	4.2.4
		[2:1]	*****000	Fixed	Must be set to Default for proper operation	
0xDF	R/W	[7]	0*******	ARC Mode Select	ARC Single Ended or Common Mode Selection, ARC Disable 0 = ARC is powered on 1 = ARC is disabled 0 = Common Mode ARC Input 1 = Single Ended ARC Input	4.5
		[6:1]	*000000*	Fixed	Must be set to Default Value	
		[0]	*******1	ARC Power Down Control	0= self bias circuit 1 = bias circuit from Irefgen 0 = ARC Powered up 1 = ARC in Power Down	4.5
0xE0	R/W	[7:0]	10000000	Fixed	Must be set to 0xD0 for proper operation	

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
0xE1	R/W	[7:0]	01111000	CEC Map Address	CEC ID I2C address for CEC I2C control map	4.1
0xE2	R/W	[3:1]	****000*	Fixed	Must be set to Default Value	
		[0]	*******0	CEC Power Down	CEC Power Down Power down CEC logic and reset CEC I2C map 0 = disabled 1 = enabled	4.9.5
0xE3	R/W	[7:1]	0000000*	Fixed	Must be set to Default Value	
0xE4	R/W	[7:2]	011000**	Fixed	Must be set to Default Value	
0xF5	RO	[7:0]	01110101	Chip ID High Byte	Chip ID High Byte	
0xF6	RO	[7:0]	00010001	Chip ID Low Byte	Chip ID Low Byte	
0xF7	RO	[7:4]	00000000	Reserved		
0xF9	R/W	[7:0]	01111100	Fixed I2C Address	This should be set to a non-conflicting I2C address	4.1
0xFA	R/W	[7:5]	000*****	Hsync Placement MSB (Embedded Sync Decoding)	This is the MSB for Hsync Placment of Embedded Sync Decoding. See Register 0x35[7:0].	4.3.7
		[4:2]	***000**	Hsync Placement MSB (Sync Adjustment)	This is the MSB for Hsync Placment of Sync Adjustment. See Register 0xD7[7:0].	4.3.7
		[1:0]	******00	Fixed	Must be default for proper operation.	4.3.7
0xFB	R/W	[7]	0*******	Hsync Delay MSB (DE Generation)	MSB for Hsync delay of DE generation. See Register 0x35[7:0]	4.3.7
		[6:5]	*00*****	Vsync Delay MSB(DE Generation)	MSB for Vsync delay of DE generation. See Register bits 0x36[5:0]	4.3.7
		[4]	***0****	Width MSB (DE Generation)	MSB for DE width of DE generation. See Register bits 0x37[4:0]	4.3.7
		[3]	****0***	Height MSB (DE Generation)	MSB for height of DE generation. See Register bits 0x39[7:0]	4.3.7
		[2:1]	*****00*	Low Refresh Rate (VIC Detection)	Low Refresh Rate indicates if input video VS refresh rate if it is less than 50Hz 00 = not low refresh rate 01 = 24Hz 10 = 25Hz 11 = 30Hz	4.3.3
0xFC	R/W	[7:6]	00******	Ri Checking Frequency	Ri Checking Frequency 00 = 128 frames 01 = 64 frames 10 = 32 frames 11 = 16 frames	4.7
		[5:3]	**000***	Ri Checking Position Delay	Ri Checking Position Delay in Units of Hsync 0 = no delay 1 = 8 Hsyncs 2 = 16 Hsyncs	4.7

Address (Main)	Type	Bits	Default Value	Register Name	Function	Reference
					3 = 32 Hsyncs 4 = 64 Hsyncs 5 = 128 Hsyncs 6 = 256 Hsyncs 7 = 512 Hsycns	
		[2:0]	*****000	BCAPS Read Delay	Delay Between Reading of BKSV and BCAPs 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms	4.7
0xFD	R/W	[7:5]	000*****	An Write Delay	Delay Between Reading of BCAPS and Writing of An 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms	4.7
		[4:2]	***000**	AKSV Write Delay	Delay Between Writing of An and Writing of AKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms	4.7
0xFE	R/W	[7:5]	000*****	HDCP Start Delay	Delay Between Setting Enable HDCP Register 0xAF[7] = 1 and Reading of BKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms	4.7

Table 112 **Packetmemory**

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0x00	R/W	[7:0]	00000000	SPD Header Byte 0		4.2.5
0x01	R/W	[7:0]	00000000	SPD Header Byte 1		4.2.5
0x02	R/W	[7:0]	00000000	SPD Header Byte 2		4.2.5
0x03	R/W	[7:0]	00000000	SPD Packet Byte 0		4.2.5
0x04	R/W	[7:0]	00000000	SPD Packet Byte 1		4.2.5
0x05	R/W	[7:0]	00000000	SPD Packet Byte 2		4.2.5
0x06	R/W	[7:0]	00000000	SPD Packet Byte 3		4.2.5
0x07	R/W	[7:0]	00000000	SPD Packet Byte 4		4.2.5
0x08	R/W	[7:0]	00000000	SPD Packet Byte 5		4.2.5
0x09	R/W	[7:0]	00000000	SPD Packet Byte 6		4.2.5
0x0A	R/W	[7:0]	00000000	SPD Packet Byte 7		4.2.5
0x0B	R/W	[7:0]	00000000	SPD Packet Byte 8		4.2.5
0x0C	R/W	[7:0]	00000000	SPD Packet Byte 9		4.2.5
0x0D	R/W	[7:0]	00000000	SPD Packet Byte 10		4.2.5
0x0E	R/W	[7:0]	00000000	SPD Packet Byte 11		4.2.5
0x0F	R/W	[7:0]	00000000	SPD Packet Byte 12		4.2.5
0x10	R/W	[7:0]	00000000	SPD Packet Byte 13		4.2.5
0x11	R/W	[7:0]	00000000	SPD Packet Byte 14		4.2.5
0x12	R/W	[7:0]	00000000	SPD Packet Byte 15		4.2.5
0x13	R/W	[7:0]	00000000	SPD Packet Byte 16		4.2.5
0x14	R/W	[7:0]	00000000	SPD Packet Byte 17		4.2.5
0x15	R/W	[7:0]	00000000	SPD Packet Byte 18		4.2.5
0x16	R/W	[7:0]	00000000	SPD Packet Byte 19		4.2.5
0x17	R/W	[7:0]	00000000	SPD Packet Byte 20		4.2.5
0x18	R/W	[7:0]	00000000	SPD Packet Byte 21		4.2.5
0x19	R/W	[7:0]	00000000	SPD Packet Byte 22		4.2.5
0x1A	R/W	[7:0]	00000000	SPD Packet Byte 23		4.2.5
0x1B	R/W	[7:0]	00000000	SPD Packet Byte 24		4.2.5

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0x1C	R/W	[7:0]	00000000	SPD Packet Byte 25		4.2.5
0x1D	R/W	[7:0]	00000000	SPD Packet Byte 26		4.2.5
0x1E	R/W	[7:0]	00000000	SPD Packet Byte 27		4.2.5
0x1F	R/W	[7]	0*******	SPD Packet Update	SPD Packet Update: Before updating the SPD Packet using I2C set to '1' to continue sending the current values. 0 = SPD Packet I2C update inactive 1 = SPD Packet I2C update active	4.2.5
0x20	R/W	[7:0]	00000000	MPEG Header Byte 0		4.3.9.2
0x21	R/W	[7:0]	00000000	MPEG Header Byte 1		4.3.9.2
0x22	R/W	[7:0]	00000000	MPEG Header Byte 2		4.3.9.2
0x23	R/W	[7:0]	00000000	MPEG Packet Byte 0		4.3.9.2
0x24	R/W	[7:0]	00000000	MPEG Packet Byte 1		4.3.9.2
0x25	R/W	[7:0]	00000000	MPEG Packet Byte 2		4.3.9.2
0x26	R/W	[7:0]	00000000	MPEG Packet Byte 3		4.3.9.2
0x27	R/W	[7:0]	00000000	MPEG Packet Byte 4		4.3.9.2
0x28	R/W	[7:0]	00000000	MPEG Packet Byte 5		4.3.9.2
0x29	R/W	[7:0]	00000000	MPEG Packet Byte 6		4.3.9.2
0x2A	R/W	[7:0]	00000000	MPEG Packet Byte 7		4.3.9.2
0x2B	R/W	[7:0]	00000000	MPEG Packet Byte 8		4.3.9.2
0x2C	R/W	[7:0]	00000000	MPEG Packet Byte 9		4.3.9.2
0x2D	R/W	[7:0]	00000000	MPEG Packet Byte 10		4.3.9.2
0x2E	R/W	[7:0]	00000000	MPEG Packet Byte 11		4.3.9.2
0x2F	R/W	[7:0]	00000000	MPEG Packet Byte 12		4.3.9.2
0x30	R/W	[7:0]	00000000	MPEG Packet Byte 13		4.3.9.2
0x31	R/W	[7:0]	00000000	MPEG Packet Byte 14		4.3.9.2
0x32	R/W	[7:0]	00000000	MPEG Packet Byte 15		4.3.9.2
0x33	R/W	[7:0]	00000000	MPEG Packet Byte 16		4.3.9.2
0x34	R/W	[7:0]	00000000	MPEG Packet Byte 17		4.3.9.2
0x35	R/W	[7:0]	00000000	MPEG Packet Byte 18		4.3.9.2

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0x36	R/W	[7:0]	00000000	MPEG Packet Byte 19		4.3.9.2
0x37	R/W	[7:0]	00000000	MPEG Packet Byte 20		4.3.9.2
0x38	R/W	[7:0]	00000000	MPEG Packet Byte 21		4.3.9.2
0x39	R/W	[7:0]	00000000	MPEG Packet Byte 22		4.3.9.2
0x3A	R/W	[7:0]	00000000	MPEG Packet Byte 23		4.3.9.2
0x3B	R/W	[7:0]	00000000	MPEG Packet Byte 24		4.3.9.2
0x3C	R/W	[7:0]	00000000	MPEG Packet Byte 25		4.3.9.2
0x3D	R/W	[7:0]	00000000	MPEG Packet Byte 26		4.3.9.2
0x3E	R/W	[7:0]	00000000	MPEG Packet Byte 27		4.3.9.2
0x3F	R/W	[7]	0*******	MPEG Packet Update	MPEG Packet Update: Before updating the MPEG Packet using I2C set to '1' to continue sending the current values. 0 = MPEG Packet I2C update inactive 1 = MPEG Packet I2C update active	4.3.9.2
0x40	R/W	[7:0]	00000000	ACP Header Byte 0		4.4.5
0x41	R/W	[7:0]	00000000	ACP Header Byte 1		4.4.5
0x42	R/W	[7:0]	00000000	ACP Header Byte 2		4.4.5
0x43	R/W	[7:0]	00000000	ACP Packet Byte 0		4.4.5
0x44	R/W	[7:0]	00000000	ACP Packet Byte 1		4.4.5
0x45	R/W	[7:0]	00000000	ACP Packet Byte 2		4.4.5
0x46	R/W	[7:0]	00000000	ACP Packet Byte 3		4.4.5
0x47	R/W	[7:0]	00000000	ACP Packet Byte 4		4.4.5
0x48	R/W	[7:0]	00000000	ACP Packet Byte 5		4.4.5
0x49	R/W	[7:0]	00000000	ACP Packet Byte 6		4.4.5
0x4A	R/W	[7:0]	00000000	ACP Packet Byte 7		4.4.5
0x4B	R/W	[7:0]	00000000	ACP Packet Byte 8		4.4.5
0x4C	R/W	[7:0]	00000000	ACP Packet Byte 9		4.4.5
0x4D	R/W	[7:0]	00000000	ACP Packet Byte 10		4.4.5
0x4E	R/W	[7:0]	00000000	ACP Packet Byte 11		4.4.5
0x4F	R/W	[7:0]	00000000	ACP Packet Byte 12		4.4.5

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0x50	R/W	[7:0]	00000000	ACP Packet Byte 13		4.4.5
0x51	R/W	[7:0]	00000000	ACP Packet Byte 14		4.4.5
0x52	R/W	[7:0]	00000000	ACP Packet Byte 15		4.4.5
0x53	R/W	[7:0]	00000000	ACP Packet Byte 16		4.4.5
0x54	R/W	[7:0]	00000000	ACP Packet Byte 17		4.4.5
0x55	R/W	[7:0]	00000000	ACP Packet Byte 18		4.4.5
0x56	R/W	[7:0]	00000000	ACP Packet Byte 19		4.4.5
0x57	R/W	[7:0]	00000000	ACP Packet Byte 20		4.4.5
0x58	R/W	[7:0]	00000000	ACP Packet Byte 21		4.4.5
0x59	R/W	[7:0]	00000000	ACP Packet Byte 22		4.4.5
0x5A	R/W	[7:0]	00000000	ACP Packet Byte 23		4.4.5
0x5B	R/W	[7:0]	00000000	ACP Packet Byte 24		4.4.5
0x5C	R/W	[7:0]	00000000	ACP Packet Byte 25		4.4.5
0x5D	R/W	[7:0]	00000000	ACP Packet Byte 26		4.4.5
0x5E	R/W	[7:0]	00000000	ACP Packet Byte 27		4.4.5
0x5F	R/W	[7]	0*******	ACP Packet Update	ACP Packet Update: Before updating the ACP Packet using I2C set to '1' to continue sending the current values. 0 = ACP Packet I2C update inactive 1 = ACP Packet I2C update active.	4.4.5
0x60	R/W	[7:0]	00000000	ISRC1 Header Byte 0		4.4.6
0x61	R/W	[7:0]	00000000	ISRC1 Header Byte 1		4.4.6
0x62	R/W	[7:0]	00000000	ISRC1 Header Byte 2		4.4.6
0x63	R/W	[7:0]	00000000	ISRC1 Packet Byte 0		4.4.6
0x64	R/W	[7:0]	00000000	ISRC1 Packet Byte 1		4.4.6
0x65	R/W	[7:0]	00000000	ISRC1 Packet Byte 2		4.4.6
0x66	R/W	[7:0]	00000000	ISRC1 Packet Byte 3		4.4.6
0x67	R/W	[7:0]	00000000	ISRC1 Packet Byte 4		4.4.6
0x68	R/W	[7:0]	00000000	ISRC1 Packet Byte 5		4.4.6
0x69	R/W	[7:0]	00000000	ISRC1 Packet Byte 6		4.4.6

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0x6A	R/W	[7:0]	00000000	ISRC1 Packet Byte 7		4.4.6
0x6B	R/W	[7:0]	00000000	ISRC1 Packet Byte 8		4.4.6
0x6C	R/W	[7:0]	00000000	ISRC1 Packet Byte 9		4.4.6
0x6D	R/W	[7:0]	00000000	ISRC1 Packet Byte 10		4.4.6
0x6E	R/W	[7:0]	00000000	ISRC1 Packet Byte 11		4.4.6
0x6F	R/W	[7:0]	00000000	ISRC1 Packet Byte 12		4.4.6
0x70	RO	[7:0]	00000000	ISRC1 Packet Byte 13		4.4.6
0x71	RO	[7:0]	00000000	ISRC1 Packet Byte 14		4.4.6
0x72	RO	[7:0]	00000000	ISRC1 Packet Byte 15		4.4.6
0x73	RO	[7:0]	00000000	ISRC1 Packet Byte 16		4.4.6
0x74	RO	[7:0]	00000000	ISRC1 Packet Byte 17		4.4.6
0x75	R/W	[7:0]	00000000	ISRC1 Packet Byte 18		4.4.6
0x76	R/W	[7:0]	00000000	ISRC1 Packet Byte 19		4.4.6
0x77	R/W	[7:0]	00000000	ISRC1 Packet Byte 20		4.4.6
0x78	R/W	[7:0]	00000000	ISRC1 Packet Byte 21		4.4.6
0x79	R/W	[7:0]	00000000	ISRC1 Packet Byte 22		4.4.6
0x7A	R/W	[7:0]	00000000	ISRC1 Packet Byte 23		4.4.6
0x7B	R/W	[7:0]	00000000	ISRC1 Packet Byte 24		4.4.6
0x7C	R/W	[7:0]	00000000	ISRC1 Packet Byte 25		4.4.6
0x7D	R/W	[7:0]	00000000	ISRC1 Packet Byte 26		4.4.6
0x7E	R/W	[7:0]	00000000	ISRC1 Packet Byte 27		4.4.6
0x7F	R/W	[7]	0*******	ISRC1 Packet Update	ISRC1 Packet Update: Before updating the ISRC1 Packet using I2C set to '1' to continue sending the current values. 0 = ISRC1 Packet I2C update inactive 1 = ISRC1 Packet I2C update active	4.4.6
0x80	R/W	[7:0]	00000000	ISRC2 Header Byte 0		4.4.6
0x81	R/W	[7:0]	00000000	ISRC2 Header Byte 1		4.4.6
0x82	R/W	[7:0]	00000000	ISRC2 Header Byte 2		4.4.6
0x83	R/W	[7:0]	00000000	ISRC2 Packet Byte 0		4.4.6

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0x84	R/W	[7:0]	00000000	ISRC2 Packet Byte 1		4.4.6
0x85	R/W	[7:0]	00000000	ISRC2 Packet Byte 2		4.4.6
0x86	R/W	[7:0]	00000000	ISRC2 Packet Byte 3		4.4.6
0x87	R/W	[7:0]	00000000	ISRC2 Packet Byte 4		4.4.6
0x88	R/W	[7:0]	00000000	ISRC2 Packet Byte 5		4.4.6
0x89	R/W	[7:0]	00000000	ISRC2 Packet Byte 6		4.4.6
0x8A	R/W	[7:0]	00000000	ISRC2 Packet Byte 7		4.4.6
0x8B	R/W	[7:0]	00000000	ISRC2 Packet Byte 8		4.4.6
0x8C	R/W	[7:0]	00000000	ISRC2 Packet Byte 9		4.4.6
0x8D	R/W	[7:0]	00000000	ISRC2 Packet Byte 10		4.4.6
0x8E	R/W	[7:0]	00000000	ISRC2 Packet Byte 11		4.4.6
0x8F	R/W	[7:0]	00000000	ISRC2 Packet Byte 12		4.4.6
0x90	R/W	[7:0]	00000000	ISRC2 Packet Byte 13		4.4.6
0x91	R/W	[7:0]	00000000	ISRC2 Packet Byte 14		4.4.6
0x92	R/W	[7:0]	00000000	ISRC2 Packet Byte 15		4.4.6
0x93	R/W	[7:0]	00000000	ISRC2 Packet Byte 16		4.4.6
0x94	R/W	[7:0]	00000000	ISRC2 Packet Byte 17		4.4.6
0x95	R/W	[7:0]	00000000	ISRC2 Packet Byte 18		4.4.6
0x96	R/W	[7:0]	00000000	ISRC2 Packet Byte 19		4.4.6
0x97	R/W	[7:0]	00000000	ISRC2 Packet Byte 20		4.4.6
0x98	R/W	[7:0]	00000000	ISRC2 Packet Byte 21		4.4.6
0x99	R/W	[7:0]	00000000	ISRC2 Packet Byte 22		4.4.6
0x9A	R/W	[7:0]	00000000	ISRC2 Packet Byte 23		4.4.6
0x9B	R/W	[7:0]	00000000	ISRC2 Packet Byte 24		4.4.6
0x9C	R/W	[7:0]	00000000	ISRC2 Packet Byte 25		4.4.6
0x9D	R/W	[7:0]	00000000	ISRC2 Packet Byte 26		4.4.6
0x9E	R/W	[7:0]	00000000	ISRC2 Packet Byte 27		4.4.6
0x9F	R/W	[7]	0*******	ISRC2 Packet Update	ISRC2 Packet Update: Before updating the ISRC2 Packet using I2C set to '1' to continue sending the current values.	4.4.6

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
					0 = ISRC2 Packet I2C update inactive 1 = ISRC2 Packet I2C update active	
0xA0	R/W	[7:0]	00000000	GM Header Byte 0		4.3.9.3
0xA1	R/W	[7:0]	00000000	GM Header Byte 1		4.3.9.3
0xA2	R/W	[7:0]	00000000	GM Header Byte 2		4.3.9.3
0xA3	R/W	[7:0]	00000000	GM Packet Byte 0		4.3.9.3
0xA4	R/W	[7:0]	00000000	GM Packet Byte 1		4.3.9.3
0xA5	R/W	[7:0]	00000000	GM Packet Byte 2		4.3.9.3
0xA6	R/W	[7:0]	00000000	GM Packet Byte 3		4.3.9.3
0xA7	R/W	[7:0]	00000000	GM Packet Byte 4		4.3.9.3
0xA8	R/W	[7:0]	00000000	GM Packet Byte 5		4.3.9.3
0xA9	R/W	[7:0]	00000000	GM Packet Byte 6		4.3.9.3
0xAA	R/W	[7:0]	00000000	GM Packet Byte 7		4.3.9.3
0xAB	R/W	[7:0]	00000000	GM Packet Byte 8		4.3.9.3
0xAC	R/W	[7:0]	00000000	GM Packet Byte 9		4.3.9.3
0xAD	R/W	[7:0]	00000000	GM Packet Byte 10		4.3.9.3
0xAE	R/W	[7:0]	00000000	GM Packet Byte 11		4.3.9.3
0xAF	R/W	[7:0]	00000000	GM Packet Byte 12		4.3.9.3
0xB0	R/W	[7:0]	00000000	GM Packet Byte 13		4.3.9.3
0xB1	R/W	[7:0]	00000000	GM Packet Byte 14		4.3.9.3
0xB2	R/W	[7:0]	00000000	GM Packet Byte 15		4.3.9.3
0xB3	R/W	[7:0]	00000000	GM Packet Byte 16		4.3.9.3
0xB4	R/W	[7:0]	00000000	GM Packet Byte 17		4.3.9.3
0xB5	R/W	[7:0]	00000000	GM Packet Byte 18		4.3.9.3
0xB6	R/W	[7:0]	00000000	GM Packet Byte 19		4.3.9.3
0xB7	R/W	[7:0]	00000000	GM Packet Byte 20		4.3.9.3
0xB8	R/W	[7:0]	00000000	GM Packet Byte 21		4.3.9.3
0xB9	R/W	[7:0]	00000000	GM Packet Byte 22		4.3.9.3
0xBA	R/W	[7:0]	00000000	GM Packet Byte 23		4.3.9.3

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0xBB	R/W	[7:0]	00000000	GM Packet Byte 24		4.3.9.3
0xBC	R/W	[7:0]	00000000	GM Packet Byte 25		4.3.9.3
0xBD	R/W	[7:0]	00000000	GM Packet Byte 26		4.3.9.3
0xBE	R/W	[7:0]	00000000	GM Packet Byte 27		4.3.9.3
0xBF	R/W	[7]	0*******	GM Packet Update	GM Packet Update: Before updating the GM Packet using I2C set to '1' to continue sending the current values. 0 = GM Packet I2C update inactive 1 = GM Packet I2C update active	4.3.9.3
0xC0	R/W	[7:0]	00000000	Spare Packet 1 Header Byte 0		4.2.7
0xC1	R/W	[7:0]	00000000	Spare Packet 1 Header Byte 1		4.2.7
0xC2	R/W	[7:0]	00000000	Spare Packet 1 Header Byte 2		4.2.7
0xC3	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 0		4.2.7
0xC4	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 1		4.2.7
0xC5	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 2		4.2.7
0xC6	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 3		4.2.7
0xC7	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 4		4.2.7
0xC8	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 5		4.2.7
0xC9	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 6		4.2.7
0xCA	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 7		4.2.7
0xCB	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 8		4.2.7
0xCC	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 9		4.2.7
0xCD	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 10		4.2.7
0xCE	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 11		4.2.7
0xCF	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 12		4.2.7
0xD0	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 13		4.2.7
0xD1	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 14		4.2.7
0xD2	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 15		4.2.7
0xD3	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 16		4.2.7
0xD4	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 17		4.2.7

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0xD5	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 18		4.2.7
0xD6	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 19		4.2.7
0xD7	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 20		4.2.7
0xD8	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 21		4.2.7
0xD9	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 22		4.2.7
0xDA	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 23		4.2.7
0xDB	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 24		4.2.7
0xDC	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 25		4.2.7
0xDD	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 26		4.2.7
0xDE	R/W	[7:0]	00000000	Spare Packet 1 Packet Byte 27		4.2.7
0xDF	R/W	[7]	0*******	Spare Packet 1 Update	Spare Packet 1 Update Before updating the Spare Packet1 using I2C set to '1' to continue sending the current values. 0 = Spare Packet 1 I2C update inactive. 1 = Spare Packet 1 I2C update active.	4.2.7
0xE0	R/W	[7:0]	00000000	Spare Packet 2 Header Byte 0		4.2.7
0xE1	R/W	[7:0]	00000000	Spare Packet 2 Header Byte 1		4.2.7
0xE2	R/W	[7:0]	00000000	Spare Packet 2 Header Byte 2		4.2.7
0xE3	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 0		4.2.7
0xE4	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 1		4.2.7
0xE5	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 2		4.2.7
0xE6	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 3		4.2.7
0xE7	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 4		4.2.7
0xE8	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 5		4.2.7
0xE9	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 6		4.2.7
0xEA	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 7		4.2.7
0xEB	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 8		4.2.7
0xEC	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 9		4.2.7
0xED	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 10		4.2.7
0xEE	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 11		4.2.7

Address (Packet Memory)	Type	Bits	Default Value	Register Name	Function	Reference
0xEF	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 12		4.2.7
0xF0	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 13		4.2.7
0xF1	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 14		4.2.7
0xF2	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 15		4.2.7
0xF3	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 16		4.2.7
0xF4	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 17		4.2.7
0xF5	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 18		4.2.7
0xF6	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 19		4.2.7
0xF7	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 20		4.2.7
0xF8	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 21		4.2.7
0xF9	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 22		4.2.7
0xFA	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 23		4.2.7
0xFB	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 24		4.2.7
0xFC	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 25		4.2.7
0xFD	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 26		4.2.7
0xFE	R/W	[7:0]	00000000	Spare Packet 2 Packet Byte 27		4.2.7
0xFF	R/W	[7]	0*******	Spare Packet 2 Update	Spare Packet 2 Update Before updating the Spare Packet 2 using I2C set to '1' to continue sending the current values. 0 = Spare Packet 2 I2C update inactive 1 = Spare Packet 2 I2C update active	4.2.7

Table 113 CEC Memory

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
0x00	R/W	[7:0]	00000000	CEC Tx Frame Header	CEC Tx Header	4.9.2
0x01	R/W	[7:0]	00000000	CEC Tx Frame Data 0	CEC Tx Opcode	4.9.2
0x02	R/W	[7:0]	00000000	CEC Tx Frame Data 1	CEC Message Operand 1	4.9.2
0x03	R/W	[7:0]	00000000	CEC Tx Frame Data 2	CEC Message Operand 2	4.9.2
0x04	R/W	[7:0]	00000000	CEC Tx Frame Data 3	CEC Message Operand 3	4.9.2
0x05	R/W	[7:0]	00000000	CEC Tx Frame Data 4	CEC Message Operand 4	4.9.2
0x06	R/W	[7:0]	00000000	CEC Tx Frame Data 5	CEC Message Operand 5	4.9.2
0x07	R/W	[7:0]	00000000	CEC Tx Frame Data 6	CEC Message Operand 6	4.9.2
0x08	R/W	[7:0]	00000000	CEC Tx Frame Data 7	CEC Message Operand 7	4.9.2
0x09	R/W	[7:0]	00000000	CEC Tx Frame Data 8	CEC Message Operand 8	4.9.2
0x0A	R/W	[7:0]	00000000	CEC Tx Frame Data 9	CEC Message Operand 9	4.9.2
0x0B	R/W	[7:0]	00000000	CEC Tx Frame Data 10	CEC Message Operand 10	4.9.2
0x0C	R/W	[7:0]	00000000	CEC Tx Frame Data 11	CEC Message Operand 11	4.9.2
0x0D	R/W	[7:0]	00000000	CEC Tx Frame Data 12	CEC Message Operand 12	4.9.2
0x0E	R/W	[7:0]	00000000	CEC Tx Frame Data 13	CEC Message Operand 13	4.9.2
0x0F	R/W	[7:0]	00000000	CEC Tx Frame Data 14	CEC Message Operand 14	4.9.2
0x10	R/W	[4:0]	***00000	CEC Tx Frame Length	CEC Tx Message Size	4.9.2
0x11	R/W	[0]	*******0	CEC Tx Transmission Enable	CEC Tx Enable 0 = Do not transmit CEC frame in Tx buffer 1 = Transmit CEC frame in Tx buffer	4.9.2
0x12	R/W	[6:4]	*001****	CEC Tx Retry	CEC Tx Retry	4.9.2
		[3:0]	****0011	CEC Tx Retry Signal Free Time	Signal Free Time Period for retransmission retry	4.9.2
0x13	R/W	[7:4]	0101****	CEC Tx SFT5	Signal Free Time of 5 periods SFT5: New initiator wants to send a frame	4.9.2
		[3:0]	****0111	CEC Tx SFT7	Signal Free Time of 7 periods SFT7: Present Initiator wants to send another frame immediately after its previous frame.	4.9.2
0x14	RO	[7:4]	0000****	CEC Tx Lowdrive Counter	Report error times in case of low impedance detection This is automatically cleared upon sending next message.	4.9.2

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
		[3:0]	****0000	CEC Tx NACK Counter	Report Error Times In Case of Negative Acknowledge	4.9.2
0x15	RO	[7:0]	00000000	CEC Rx Buffer 1 Frame Header	Rx Header Block in the Frame (Buffer 1)	4.9.3
0x16	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 0	Rx Data Opcode (Buffer 1)	4.9.3
0x17	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 1	Received CEC Operand 1(Buffer 1)	4.9.3
0x18	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 2	Received CEC Operand 2 (Buffer 1)	4.9.3
0x19	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 3	Received CEC Operand 3 (Buffer 1)	4.9.3
0x1A	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 4	Received CEC Operand 4 (Buffer 1)	4.9.3
0x1B	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 5	Received CEC Operand 5 (Buffer 1)	4.9.3
0x1C	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 6	Received CEC Operand 6 (Buffer 1)	4.9.3
0x1D	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 7	Received CEC Operand 7 (Buffer 1)	4.9.3
0x1E	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 8	Received CEC Operand 8 (Buffer 1)	4.9.3
0x1F	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 9	Received CEC Operand 9 (Buffer 1)	4.9.3
0x20	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 10	Received CEC Operand 10 (Buffer 1)	4.9.3
0x21	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 11	Received CEC Operand 11 (Buffer 1)	4.9.3
0x22	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 12	Received CEC Operand 12 (Buffer 1)	4.9.3
0x23	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 13	Received CEC Operand 13 (Buffer 1)	4.9.3
0x24	RO	[7:0]	00000000	CEC Rx Frame Buffer 1 Data byte 14	Received CEC Operand 14 (Buffer 1)	4.9.3
0x25	RO	[4:0]	***00000	CEC Rx Buffer 1 Frame Length	Rx Message Size (Buffer 1) Number of operands + 2	4.9.3
0x26	RO	[6]	*1******	CEC Rx Enable	RX enable 0 = The CEC module is currently not able to	4.9.3

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
					receive a new CEC frame 1 = The CEC module is currently able to receive a new CEC frame	
		[5:4]	**00****	CEC Rx Buffer 3 Timestamp	Specifies the order in which the message in Buffer 3 was received relative to Buffer 1 and Buffer 2 for the current buffered messages 00 = No valid message 01 = Oldest received buffered message 10 = Second most Recent received buffered message 11 = Most Recent received buffered message	4.9.3
		[3:2]	****00**	CEC Rx Buffer 2 Timestamp	Specifies the order in which the message in Buffer 2 was received relative to Buffer 1 and Buffer 3 for the current buffered messages 00 = No valid message 01 = Oldest received buffered message 10 = Second most Recent received buffered message 11 = Most Recent received buffered message	4.9.3
		[1:0]	******00	CEC Rx Buffer 1 Timestamp	Specifies the order in which the message in Buffer 1 was received relative to Buffer 2 and Buffer 3 for the current buffered messages 01 = Oldest received buffered message 10 = Second most Recent received buffered message 11 = Most Recent received buffered message	4.9.3
0x27	RO	[7:0]	00000000	CEC Rx Buffer 2 Frame Header	Rx Header Block in the Frame (Buffer 2)	4.9.3
0x28	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 0	Rx Data Opcode (Buffer 2)	4.9.3
0x29	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 1	ReceivedCEC Operand 1(Buffer 2)	4.9.3
0x2A	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 2	ReceivedCEC Operand 2 (Buffer 2)	4.9.3
0x2B	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 3	Received CEC Operand 3 (Buffer 2)	4.9.3
0x2C	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 4	Received CEC Operand 4 (Buffer 2)	4.9.3
0x2D	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 5	Received CEC Operand 5 (Buffer 2)	4.9.3
0x2E	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 6	Received CEC Operand 6 (Buffer 2)	4.9.3
0x2F	RO	[7:0]	00000000	CEC Rx Frame Buffer 2	Received CEC Operand 7 (Buffer 2)	4.9.3

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
				Data byte 7		
0x30	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 8	Received CEC Operand 8 (Buffer 2)	4.9.3
0x31	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 9	Received CEC Operand 9 (Buffer 2)	4.9.3
0x32	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 10	Received CEC Operand 10 (Buffer 2)	4.9.3
0x33	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 11	Received CEC Operand 11 (Buffer 2)	4.9.3
0x34	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 12	Received CEC Operand 12 (Buffer 2)	4.9.3
0x35	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 13	Received CEC Operand 13 (Buffer 2)	4.9.3
0x36	RO	[7:0]	00000000	CEC Rx Frame Buffer 2 Data byte 14	Received CEC Operand 14 (Buffer 2)	4.9.3
0x37	RO	[4:0]	***00000	CEC Rx Buffer 2 Frame Length	Rx Message Size (Buffer 2) Number of operands + 2	4.9.3
0x38	RO	[7:0]	00000000	CEC Rx Buffer 3 Frame Header	Rx Header Block in the Frame (Buffer 3)	4.9.3
0x39	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 0	Rx Data Opcode (Buffer 3)	4.9.3
0x3A	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 1	Received CEC Operand 1(Buffer 3)	4.9.3
0x3B	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 2	Received CEC Operand 2 (Buffer 3)	4.9.3
0x3C	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 3	Received CEC Operand 3 (Buffer 3)	4.9.3
0x3D	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 4	Received CEC Operand 4 (Buffer 3)	4.9.3
0x3E	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 5	Received CEC Operand 5 (Buffer 3)	4.9.3
0x3F	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 6	Received CEC Operand 6 (Buffer 3)	4.9.3
0x40	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 7	Received CEC Operand 7 (Buffer 3)	4.9.3
0x41	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 8	Received CEC Operand 8 (Buffer 3)	4.9.3

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
0x42	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 9	Received CEC Operand 9 (Buffer 3)	4.9.3
0x43	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 10	Received CEC Operand 10 (Buffer 3)	4.9.3
0x44	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 11	Received CEC Operand 11 (Buffer 3)	4.9.3
0x45	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 12	Received CEC Operand 12 (Buffer 3)	4.9.3
0x46	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 13	Received CEC Operand 13 (Buffer 3)	4.9.3
0x47	RO	[7:0]	00000000	CEC Rx Frame Buffer 3 Data byte 14	Received CEC Operand 14 (Buffer 3)	4.9.3
0x48	RO	[4:0]	***00000	CEC Rx Buffer 3 Frame Length	Rx Message Size (Buffer 3) Number of operands + 2	4.9.3
0x49	RO	[2]	*****0**	CEC Rx Buffer 3 Ready	Indicates frame presence in Buffer 3 0 = No CEC frame available in buffer 3 1 = A CEC frame is available in buffer 3	4.9.3
		[1]	******0*	CEC Rx Buffer 2 Ready	Indicates frame presence in Buffer 2 0 = No CEC frame available in buffer 2 1 = A CEC frame is available in buffer 2	4.9.3
		[0]	*******0	CEC Rx Buffer 1 Ready	Indicates frame presence in Buffer 1 0 = No CEC frame available in buffer 1 1 = A CEC frame is available in buffer 1	4.9.3
0x4A	R/W	[3]	****1***	Use all CEC Rx Buffers	Choose whether the new frames should be received in all 3 buffers or only one buffer 0 = Use only buffer 0 to store CEC frames (Legacy mode) 1 = Use all 3 buffers to stores the CEC frames (Non-legacy mode)	4.9.3
		[2]	*****0**	CEC Rx Buffer 3 Ready Clear	Set high to clear 0x49[2] and reset 0x26[5:4] 0 = Retain the value of 0x49[2] 1 = Clear out 0x49[2]	4.9.3
		[1]	******0*	CEC Rx Buffer 2 Ready Clear	Set high to clear 0x49[1] and reset 0x26[3:2] 0 = Retain the value of 0x49[1] 1 = Clear out 0x49[1]	4.9.3
		[0]	*******0	CEC Rx Buffer 1 Ready Clear	Set high to clear 0x49[0] and reset 0x26[1:0] 0 = Retain the value of 0x49[0] 1 = Clear out 0x49[0]	4.9.3
0x4B	R/W	[6:4]	*001****	Logical Address Mask	Logical Address Mask of the CEC Devices: Supports up to 3 logical devices. When the bit is one, the related logical device will be enabled, and the messages whose destination	4.9.5

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
					address is matched with the logical address will be accepted 001 = mask bit for logical device0 010 = mask bit for logical device1 100 = mask bit for logical device2	
		[3]	****0***	Error Report Mode	Error report mode 0 = only report short bit period error 1 = report both short and long bit period errors	4.9.5
		[2]	*****0**	Error Detect Mode	Error Detect Mode If an error is detected, CEC controller will drive the CEC line low for 3.6msec immediately to notify the line error to the initiator 0 = any short bit period except start bit 1 = only when destination is broadcast	4.9.5
		[1]	******0*	Force NACK	Force NACK. If this bit is set, CEC Rx module will NACK any message. 0 = ACK the relevant messages 1 = NACK all messages	4.9.5
		[0]	*******0	Force Ignore	If this bit is set, CEC Rx module will ignore any directly addressed message belonging to it. 0 = ACK the relevant messages 1 = NACK all messages	4.9.5
0x4C	R/W	[7:4]	1111****	Logical Address 1	Logical Address of logical device 1	4.9.5
		[3:0]	****1111	Logical Address 0	Logical Address of logical device 0	4.9.5
0x4D	R/W	[3:0]	****1111	Logical Address 2	Logical Address of logical device 2	4.9.5
0x4E	R/W	[7:2]	001111**	CEC Clock Divider	CEC Clock Divider: The input clock frequency is divided according to the value in this register. The divided clock is used as the CEC process clock. Internal clock frequency = input clock frequency / (clock_divider+1) 000000 = no division and the input clock will be used as the CEC process clock directly 000001 = divide by 2 000010 = divide by 3 000011 = divide by 4 111110 = divide by 63 111111 = divide by 64	4.9.5
		[1:0]	******00	CEC Power Mode	Power mode of CEC. Does not reset I2C map on power down. 00 = Completely Power Down	4.9.5

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
					01 = Always Active 10 = Depend on HPD status 11 = Depend on HPD status	
0x4F	R/W	[5:0]	**000111	Glitch Filter Ctrl	Glitch filter control for the CEC input: The CEC bus is sampled by the input clock. This Register indicates the number of clock cycles. Pulses whose width is less than the value in this register will be filtered by the CEC module. 000000 = filter is disabled 000001 = pulse width less than 1 clock cycle will be filtered. 111111 = pulse width less than 63 will be filtered	4.9.5
0x50	R/W	[0]	*******0	CEC Soft Reset	CEC reset by external host 0 = Do not reset CEC controller 1 = Reset CEC controller	4.9.5
0x51	R/W	[15:0]	00001101	St Total	CEC nominal start bit total period. Typically it is 4.5ms Typical value at 750KHz	4.9.5
0x52			00101111			
0x53	R/W	[15:0]	00001100	St Total Min	CEC minimum start bit total period. Typically, it is 4.3ms, for the default value, keep 0.1ms margin, namely 4.2ms Typical value at 750KHz	4.9.5
0x54			01001110			
0x55	R/W	[15:0]	00001110	St Total Max	CEC maximum start bit total period. Typically, it is 4.7ms, for the default value, keep 0.1ms margin, namely 4.8ms Typical value at 750KHz	4.9.5
0x56			00010000			
0x57	R/W	[15:0]	00001010	St Low	CEC nominal start bit low period. Typically it is 3.7ms Typical value at 750KHz	4.9.5
0x58			11010111			
0x59	R/W	[15:0]	00001001	St Low Min	CEC minimum start bit low period. Typically it is 3.5ms, for the default value, keep 0.1ms margin, namely 3.4ms Typical value at 750KHz	4.9.5
0x5A			11110110			
0x5B	R/W	[15:0]	00001011	St Low Max	CEC maximum start bit low period. Typically it is 3.9ms, for the default value, keep 0.1ms margin, namely 4.0ms Typical value at 750KHz	4.9.5
0x5C			10111000			
0x5D	R/W	[15:0]	00000111	Bit Total	CEC nominal data bit total period. Typically it is 2.4ms. Typical value at 750KHz	4.9.5
0x5E			00001000			
0x5F	R/W	[15:0]	00000101	Bit Total Min	CEC minimum data bit low period. Typically it is 2.05ms, for the default value, keep 0.1ms margin, namely 1.95ms	4.9.5
0x60			10110111			

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
					Typical value at 750KHz	
0x61	R/W	[15:0]	00001000	Bit Total Max	CEC maximum data bit low period. Typically it is 2.75ms, for the default value, keep 0.1ms margin, namely 2.85ms Typical value at 750KHz	4.9.5
0x62			01011010			
0x63	R/W	[15:0]	00000001	Bit Low One	CEC nominal data bit low period for logical 1. Typically it is 0.6ms Typical value at 750KHz	4.9.5
0x64			11000010			
0x65	R/W	[15:0]	00000100	Bit Low Zero	CEC nominal data bit low period for logical 0. Typically it is 1.5ms Typical value at 750KHz	4.9.5l
0x66			01100101			
0x67	R/W	[15:0]	00000101	Bit Low Max	CEC nominal data bit low period for logical 0. Typically it is 1.8ms Typical value at 750KHz	4.9.5
0x68			01000110			
0x69	R/W	[15:0]	00000011	Sample Time	CEC nominal sample time. Typically it is 1.05ms Typical value at 750KHz	4.9.5
0x6A			00010011			
0x6B	R/W	[15:0]	00001010	Line Error Time	CEC Line Error handling time. Typically it is 1.4~1.6 times the nominal data bit period. We set the default value to 1.5 times the nominal data bit period.	4.9.5
0x6C			10001100			
0x6D	R/W	[0]	*******0	Fixed	Must be default for proper operation	.
0x6E	R/W	[15:0]	00000000	Rise Time	CEC maximum rise time. Typically it is 250us	4.9.5
0x6F			10111100			
0x70	R/W	[0]	*******0	Bit Low Detmode	Error detection mode for data bit low period 0 = Disabled 1 = Enable	4.9.5
0x71	R/W	[15:0]	00000000	Bit Low One Min	CEC minimum data bit low period for logical 1. Typically it is 0.4ms, for the default value, keep 0.1ms margin, namely 0.3ms Typical value at 750KHz	4.9.5
0x72			11100001			
0x73	R/W	[15:0]	00000010	Bit Low One Max	CEC maximum data bit low period for logical 1. Typically it is 0.8ms, for the default value, keep 0.1ms margin, namely 0.9ms Typical value at 750KHz	4.9.5
0x74			10100011			
0x75	R/W	[15:0]	00000011	Bit Low Zero Min	CEC minimum data bit low period for logical 0. Typically it is 1.3ms, for the default value, keep 0.1ms margin, namely 1.2ms Typical value at 750KHz	4.9.5
0x76			10000100			
0x77	R/W	[7:0]	01101101	Wake Up Opcode 1	Wake up opcode 0 -> When detected and a response is needed, the MPU is woken up	4.9.5

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
					through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Power On' opcode	
0x78	R/W	[7:0]	10001111	Wake Up Opcode 2	Wake up opcode 1 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Give Power Status' opcode	4.9.5
0x79	R/W	[7:0]	10000010	Wake Up Opcode 3	Wake up opcode 2 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Active Source' opcode	4.9.5
0x7A	R/W	[7:0]	00000100	Wake Up Opcode 4	Wake up opcode 3 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Image View On' opcode	4.9.5
0x7B	R/W	[7:0]	00001101	Wake Up Opcode 5	Wake up opcode 4 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Text View On' opcode	4.9.5
0x7C	R/W	[7:0]	01110000	Wake Up Opcode 6	Wake up opcode 5 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'System Audio Mode Request' opcode	4.9.5
0x7D	R/W	[7:0]	01000010	Wake Up Opcode 7	Wake up opcode 6 -> When detected and a	4.9.5

Address (CEC)	Type	Bits	Default Value	Register Name	Function	Reference
					response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Deck Control' opcode	
0x7E	R/W	[7:0]	01000001	Wake Up Opcode 8	Wake up opcode 7 -> When detected and a response is needed, the MPU is woken up through an interrupt. Upon receiving this code an interrupt in generated. User can pre-define the opcode in their application to automatically generate interrupt upon individual opcode. Default set at 'Play' opcode	4.9.5
0x7F	R/W	[7]	1*******	CDC Arbitration Enable	Controls whether to do special CDC messsage arbitration upon receiving CDC messsage 1 = enable 0 = disable	4.9.5
		[6]	*1******	CDC HPD Response Enable	Controls whether to toggle internal HPD signals when receving CDC HPD messsage 1 = enable 0 = disable	4.2.1 4.9.5
0x80 0x81	R/W	[15:0]	00000000 00000000	CEC Physical Address	Physical address of CEC device	4.2.1 4.9.5
0x82	R/W	[7:0]	00000001	CDC HPD Timer Count	Controls the time CDC HPD stays low when receiving CDC HPD toggle message. HPD low = CDC_HPD_Timer_Count * CEC_CLK. CEC_CLK is 760KHz by default.	4.2.1 4.9.5
0x83	RO	[7]	0*******	CDC HPD	HPD signal from CEC interface	4.2.1 4.9.5
0xC0 0xC1	R/W	[11:0]	****0000 00000000	Y or RGB Minimum	Minumum value for Y or RGB for video data clipping.	4.3.8
0xC2 0xC3	R/W	[11:0]	****1111 11111111	Y or RGB Maximum	Maximum value for Y or RGB for video data clipping.	4.3.8
0xC4 0xC5	R/W	[11:0]	****0000 00000000	CbCr Minimum	Minimum value for Cb/Cr for video data clipping	4.3.8
0xC6 0xC7	R/W	[11:0]	****1111 11111111	CbCr Maximum	Maximum value for Cb/Cr for video data clipping.	4.3.8